INVESTIGATION OF INTERFACE STATES AND RADIATION DEFECTS IN $Si/SiO_2/In_2O_3$ (E-Beam Deposited) STRUCTURES BY OPTICAL MOS ADMITTANCE TECHNIQUE

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AUGUST, 1985

CERTIFICATE

This is to certify that the work entitled, INVESTIGATION OF INTERFACE STATES AND RADIATION DEFECTS IN $Si/SiO_2/In_2O_3$ (E-BEAM DEPOSITED) STRUCTURES BY OPTICAL MOS ADMITTANCE TECHNIQUE, by Mr. Harwesh Bhatiya, has been carried out under my supervision and has not been submitted elsewhere for a degree.

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Harwesh Bhatiya

CONTENTS

ABSTRACT

The aim of the present work is to investigate the damages induced in the MOS structure because of the Electron-Beam irradiation. For this purpose $Si/SiO_2/In_2O_3$ structure whose top transparent gate was deposited employing Electron-Beam evaporation was studied and the analysis done by both the capacitance and the conductance technique to determine the interface state density profile. A uniform background of illumination was provided so as to access the minority carrier band gap half also for the purpose of interface state density and the capture cross section determination.

The peak, induced due to the damages caused by the Electron-Beam irradiation was found to be approximately in the energy range of 0.8 - 0.95 eV above the valence band edge and the magnitude and the position of the peak was found to shift with the varying illumination level.

CHAPTER I

INTRODUCTION

Exposure to some radiation process is a very common phenomenon in the steps involved to fabricate various semiconductor devices including MOS. Reactive Ion Etching, Ion Implantation, Electron Beam Evaporation and Lithography are some of such processes.

In the case of MOS this irradiation introduces defects such as build up of fixed positive charges near the $Si-SiO_2$ interface which manifests itself by causing a small shift in the ideal C-V curve of the MOS along the voltage scale [1]. The irradiation also causes creation of fast surface states at the $Si-SiO_2$ interface.

Physically three different processes may give rise to the damages produced in the device due to irradiation [2]. These are firstly atomic displacement in which high energy massive particles transfer their energy to the Si-O network by physically knocking away a network atom, tearing aside it's bond, secondly primary ionization in which ionizing radiation transfers its energy to the Si-O network by exciting bonding electrons and creating free electrons and holes and thirdly secondary ionization which is caused by the electrons produced in the first two processes.

In our work we are concerned with the effect of Electron Beam radiation on the interface states and the defects introduced due to this radiation in $Si/SiO_2/In_2O_3$ structures.

Out of the three damaging processes described above the first one is obviously not involved in the case of E-Beam deposition of the top metallization because of very small momentum of the particles, the mass of an electron being negligibly small.

Although the defects introduced in the device due to E-Beam radiation can be annealed out by a suitable annealing process to a large extent for our purpose no post metallization annealing was carried out.

The interface states play a very important role in the operation of an MOS device. Being electrically active their charging and discharging contributes towards the capacitance of the device and this capacitance varies with the applied bias as the density of interface states has a certain distribution in the band gap of the Silicon. This distribution over energy in the band gap has been found to depend upon the oxide thickness of the MOS for thickness less than 300 Å and seems to be related to the mechanism of oxide growth [3].

Optical illumination was employed in the present work because illumination dependence of the interface state distribution in the bond gap and various characteristics of MOS are of

importance in Optoelectronics. Besides this there are several other advantages of employing optical illumination technique. Capture cross section of electrons, σ_e, in the upper band gap half and hole capture cross section, σ_n, in the lower band gap half can be obtained, if the device is illuminated. We know that even in inversion regime the interface states are expected to exchange charge with the majority carrier band only under dark condition, consequently the interface states which are closer to the minority carrier band edge can not be accessed in the dark, but with illumination provided these states can be accessed as they can now exchange charge with the minority carrier band in the inversion regime [4].

Thus optical illumination technique is a very powerful tool to obtain interface state density over most of the band gap very accurately by taking measurements under various illumination intensities.

Advantage of using Electron Beam evaporation for the deposition of tin doped indium oxide is the lower sheet resistivity thus obtained so as to reduce the series resistance of the device and thereby reducing the inaccuracies in conductance measurement of the device.

Tin doped indium oxide was chosen as the transparent gate because of its good adhesion, durability, chemical stability and ease of deposition [5].

In the present work, therefore we have undertaken to investigate the effects of Electron-Beam radiation on interface state density distribution and the defects produced because of this radiation in the device which in our work is the $Si/SiO_2/In_2O_3$ structure whose top metallization of In_2O_3 was fabricated using Electron-Beam evaporation. In the second chapter the theory of $Si-SiO_2$ interface with respect to its characteristics and origin of interface states has been given along with the various methods used to determine the interface states distribution in the band gap. The third chapter describes the fabrication of the device and the measurement setup. Analysis and results have been presented in Chapter Four and finally the conclusions drawn out of the study carried out.

REFERENCES

1. H.S. Lee, IEEE Transactions on Elect. Devices, Vol.ED-25, No. 7, July 1978, pp. 795-799.
2. R.A. Gdula, IEEE Transactions on Electron Devices, Vol. ED-26, No.4, April 1979, pp. 644-647.
3. S.Kar, D. Shanker, K.S. Chari, to be published.
4. S.Kar, S. Varma, to be published
5. S.Kar, S. Varma and P. Saraswat, J. Appl.Phys.53, 7039 (1982).

CHAPTER II

INTERFACE INVESTIGATION THEORY AND PROCEDURE

2.1 Ideal and Practical Silicon-Silicondioxide Interface

When an oxide layer is thermally grown over a Si wafer the various types of trap states and charges associated with it are the interface trapped charge, fixed charge, oxide trapped charge and the mobile charge.

The interface trapped charges are located at the interface and have energy states in the silicon band gap and can interact electrically with the underlying silicon. Hence an understanding of the origin of such states, their density and distribution in the forbidden energy gap is of utmost importance. Most of the unannealed MOS capacitors are reported to exhibit an interface state density profile consisting of two peaked distributions, one close to the valence band maximum and the other close to the conduction band minimum overlying a concave background. The peaked distribution have been attributed to non-stoichiometry at the interface and mostly disappear on annealing leaving behind a U-shaped profile [1].

Regarding the origin of the interface states various model have been proposed in the past studies. Sakurai and Sugano [2] developed a calculation method based on semi-empirical tight

binding Hamiltonians and the Green's function formulation and applied for calculation of the energy level of the trap states between amorphous SiO_2 and the silicon substrate and concluded that the perfect interface does not have any states in the forbidden gap of Si although the Si-O-Si bonding angle at the interface is varied in the range between 120° and 180° and neither does the interface with oxygen dangling bonds have any states.

The three types of models which can give rise to an interface state in the energy band gap are shown in the Figs. 2.1(b), (c) and (d). The trap states existing due to silicon dangling bonds as shown in (b) appear at about the middle of the band gap. Existence of the states in the energy range higher than the midgap are a result of the contribution from O-vacancy and Si-Si weak bonds at the interface as shown in (c) and finally the Si-O weak bonds at the interface produce trap states in the lower band gap half Fig. (d).

The energy level of these states is a function of bonding parameters such as bond lengths and angles.

Experimental work by Pointdexter and others [3] involving Electron Paramagnetic Resonance (EPR) have revealed a P_b center, which is a major characteristic defect of the $Si-SiO_2$ interface, and has been identified as a triply coordinated silicon atom with a dangling orbital. They further examined [4] some samples

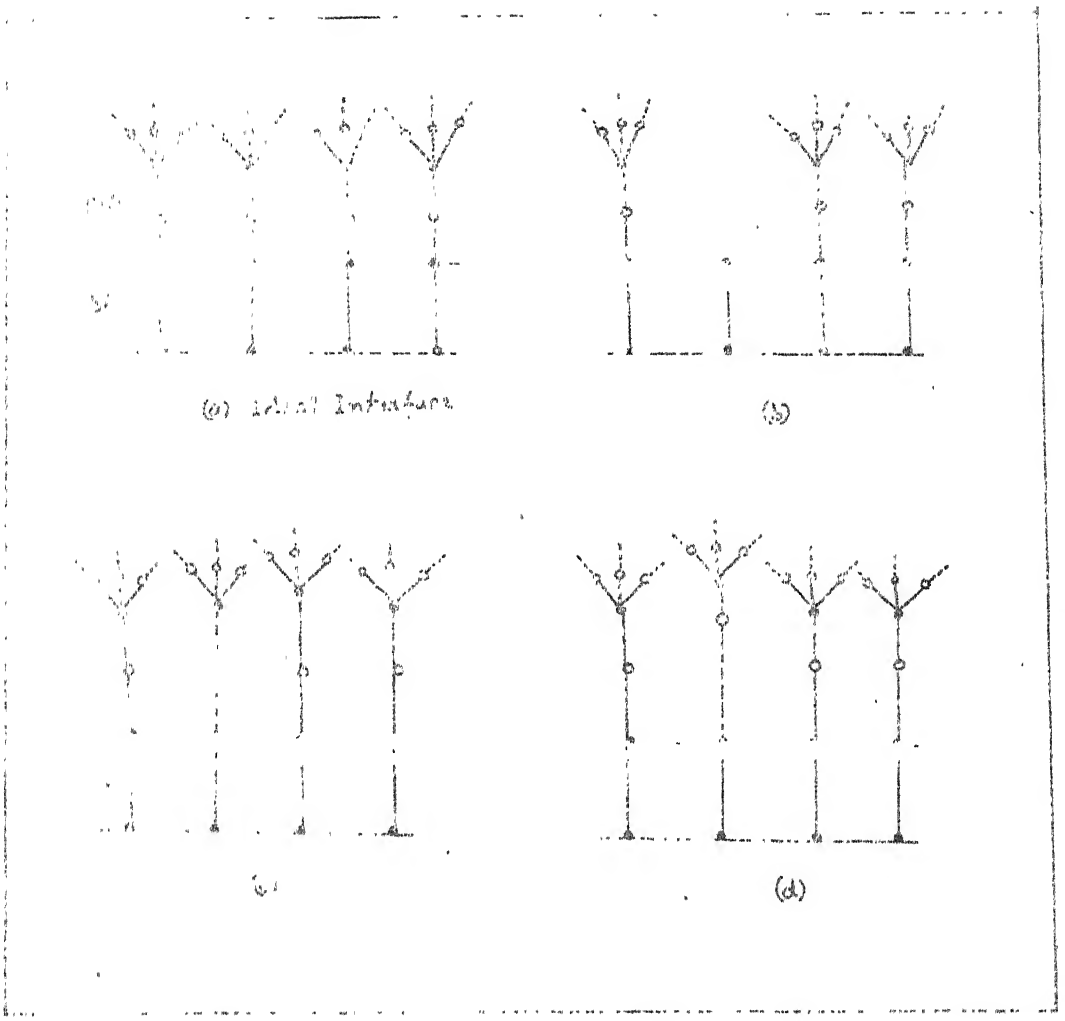

Fig. 2.1: Ideal and Damaged Silicon-Silicondioxide Interface.

by EPR as well as C-V analysis and the P_b center profile thus obtained had a good correlation in peak position and peak value of density with the interface state profile indicating that the silicon dangling bond is the cause for the interface states in as oxidized samples.

The fixed oxide charge, as the name suggests are not electrically active and they can not be charged or discharged with a bias applied to the device, they can only cause a parallel shift in the C-V curves along the voltage axis. The fixed oxide charges are positive and located in the oxide within approximately 30 Å of the silicon layer in the transition layer. These charges arise due to structural defect in the transition region and their density ranges from $10^{10}/cm^2$ to $10^{12}/cm^2$ which depends upon oxidation and annealing conditions as well as on the substrate orientation. Another type of charges present in a silicondioxide - silicon system are the oxide trapped charges which are due to the holes or, electrons trapped in the bulk of the oxide. These charges are associated with the defects in the oxide resulting from processing techniques such as E-Beam Evaporation, E-Beam or X-Ray Lithography, Ion-Implantation, Plasma or Reactive Ion Etching, and Ion Beam Milling etc. used in the fabrication of VLSI circuits. The trapped charges also like fixed charges give rise to a shift in the capacitance voltage characteristics of an MOS device parallel to the voltage axis. The density of these charges

vary from 10^9 cm^{-2} to 10^{13} cm^{-2} and they can be removed by annealing [5].

The mobile charges which are generally alkali ions such as sodium and potassium ions get into the oxide mainly due to contamination in processing materials, chemicals, ambient and handling. Cleaning the furnace in chlorine ambient and gettering in phosphosilicate glass and the use of chlorine or HCl in the oxidation ambient reduces this charge, which ranges from $10^{10}/cm^2$ to $10^{12}/cm^2$.

These ions are mobile even at room temperature when electric field is present hence cause drift.

2.2 Interface Investigation Techniques

Various experimental techniques have been developed for interface investigation of MOS structures. For large interface state density high frequency method of Terman [6] can be adopted but this method is quite unreliable because of the uncertainty about the magnitude of the semi-conductor space charge capacitance A more reliable low frequency method was suggested by Bergland [7] The quasi-static method proposed by Kuhn [8] combines measurement of low and high frequency capacitance. But the leakage current in thin oxides being large creates a problem. The only method which gives an accurate determination of the interface state density and their capture cross sections was the a.c. conductance method proposed by Nicollian and Goitzberger [9].

Recently the a.c. conductance technique has been extended to the case of admittance measurements in a uniform background of optical illumination [10,11,12]. The low frequency capacitance method also can be used with illumination [13] and the difficulties encountered in that can be over come by using the admittance method along with this.

2.2.1 Low Frequency Capacitance Method

The principle of determining the interface state density employing low frequency capacitance method can be explained with the help of the low frequency equivalent circuit of the MOS capacitor shown in the Fig. 2.2.

At low frequencies the interface state branch of the equivalent circuit consists of C_{is} only as the reactance due to C_{is} at low frequencies is very large as compared to R_{is}.

Hence if C_{ox} is known, C^{p}_{lf} can be calculated from the measured C_{lf} and C_{is} can be extracted from it as C^{p}_{lf} is the sum of C_{sc} and C_{is}, C_{sc} being known in terms of interface potential as per the following equation [9].

$$C_{sc}/A = (\varepsilon_s/L_D)[1-\exp(-U_s) + (n_{po}/p_{po})\ (\exp U_s - 1)]/$$
$$F(U_s,\ n_{po}/p_{po}),\ p - Si \qquad (2.1)$$

where $F(U_s,\ n_{po}/p_{po}) = [\exp(-U_s)+U_s-1 + (n_{po}/p_{po})(\exp U_s-U_s-1)]^{1/}$

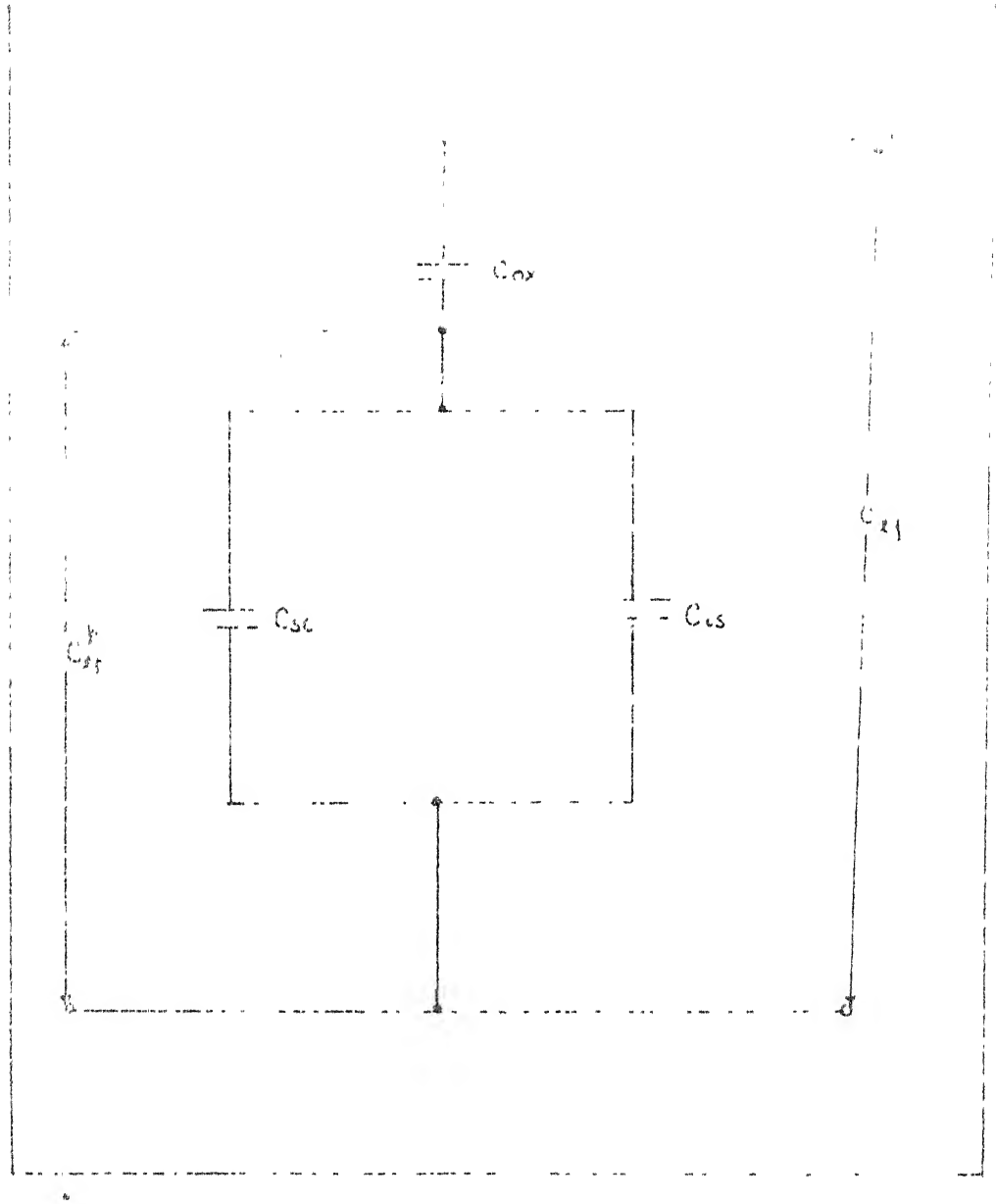

Fig. 2.2: ow Frequency Equivalent Circuit of MOS.

This equation is valid for dark condition only and for illumination this will have to be modified by introducing Fermi level separation ΔE_F in the above equation.

This equation under illumination is [1]

$$C_{scl} = (\varepsilon_s/L_D)\,[1 - \exp(-U_s) + (n'_{po}/p'_{po})\,(\exp(U_s) - 1)]/F(U_s, n'_{po}/p'_{po})$$

where,

$$p'_{po} = p_{po} = N_A \qquad (2.2)$$

$$n'_{po} = n_{po} \exp(\Delta E_F/kT)$$

The interface states are observed to be comprised of many levels so closely spaced in energy that they can not be distinguished as separate levels. For a continuum of interface states at a finite temperature, capture and emission of carriers can occur by states located within a kT/q of the Fermi level. The admittance of this continuum is then got by integration. If N_{ss} and C_p do not vary much over kT/q energy range, the equivalent parallel capacitance and conductance are given by the relations [9].

$$\text{(a)} \quad C_p(\omega) = C_{sc} + q N_{ss} \frac{\tan^{-1}\omega\tau}{\omega\tau} \qquad (2.3)$$

$$\text{(b)} \quad G_p(\omega) = \frac{qN_{ss}}{2} \cdot \frac{1+\omega^2\tau^2}{\tau}$$

At low frequencies the equivalent parallel capacitance reduces to

$$C_p(\omega) = C_{sc} + q N_{ss} = C_{sc} + C_{ss} \qquad (2.4)$$

While plotting the interface state density profile it's necessary to know the energy position of the states in the band gap corresponding to a certain interface potential. In the case of dark it can be found out very easily as the interface states exchange charge with the majority carriers only and hence the position in the band gap can be obtained by the following equation

$$E-E_v = q(\phi_p + \phi_i) \qquad (2.5)$$

Under illumination since two quasi Fermi levels are existing in the band gap interface states exchange charge with that carrier band which at the $Si-SiO_2$ interface is closer to its corresponding quasi Fermi level as compared to other band edge assuming the capture cross-sections of both holes and electrons to be equal. Therefore, in case of p-type samples if charge exchange takes place with majority carrier band

$$E-E_v = q(\phi_p + \phi_i) \qquad (2.6a)$$

and if with minority carrier band

$$E-E_v = q(\phi_p + \phi_i + \Delta E_F) \qquad (2.6b)$$

2.2.2 Conductance Technique

In this method conductance part of the total admittance consisting of oxide capacitance, space charge capacitance and the interface state admittance is made use of to get the information about the interface states. The interface states admittance arises due to the charge exchange between the interface states and the silicon energy bands. In the dark it is not possible to study the interface states near the minority carrier band edge because the minority carrier concentration does not follow the applied signal as they have to be thermally generated which has a longer time constant, so the interface state conductance is determined solely by the charge exchange with the majority carrier band.

In the case of optical illumination with photon energy in excess of silicon energy gap, minority carriers can be supplied by the photogeneration of electron-hole pairs. Hence the interface states can exchange charge with either of the carrier bands and the relative or dominant contribution of these bands will depend primarily on the relative ease of electron and hole capture.

The interface states may occur as a single level state or as a continuum of states. The MOS capacitor can be then represented by the equivalent circuit of Fig. 2.3 as shown.

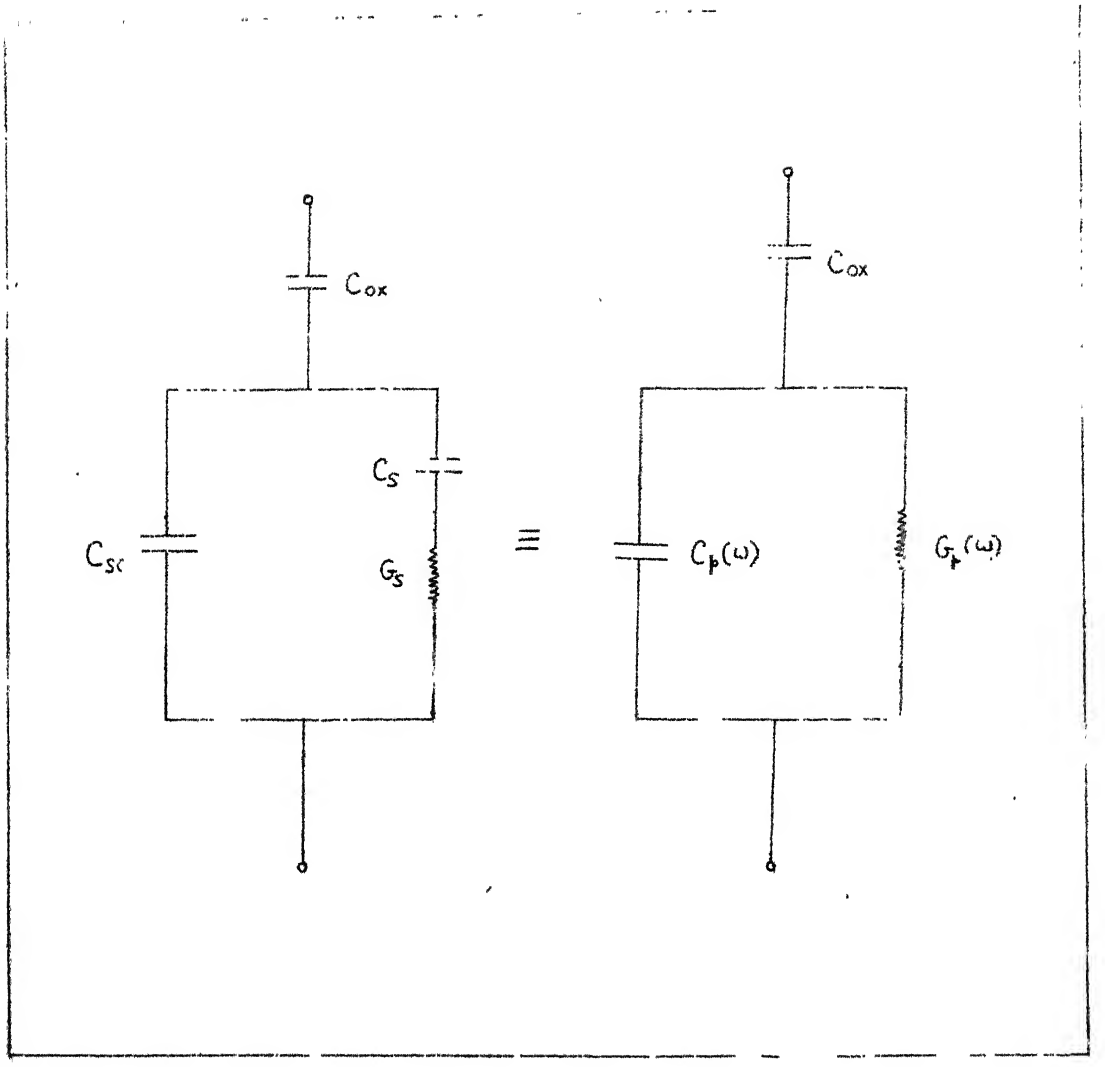

Fig. 2.3: Equivalent Circuit of an MOS Capacitor with a Continuum of States at the Interface.

The equivalent parallel conductance $G_p(\omega)$ in the case of single level and continuum of states in terms of C_s, ω and interface time constant τ are given by the following relations [9].

Single Level State: $$G_p(\omega) = \frac{C_s \omega^2 \tau}{1 + \omega^2 \tau^2}$$

Continuum of States: $$G_p(\omega) = \frac{C_s}{2} \cdot \frac{\ln (1 + \omega^2 \tau^2)}{\tau} \qquad (2.7)$$

It can be observed from the above relations that G_p/ω goes through a maximum in both the cases and the maximum value is directly proportional to the interface state capacitance and hence interface state density.

In the case of a single level state the peak in G_p/ω curve occurs when $\omega\tau = 1$ and the peak value of G_p/ω is equal to $C_{is}/2$ as can be seen from the equation. When a continuum of states exist in the band gap G_p/ω goes through a maximum when $\omega\tau = 1.98$ and we have the following relations [9]

$$(G_p/\omega)_{max} = \frac{q.A.N_{ss}}{2} \cdot 0.805$$

and thus,

$$N_{ss} = 1.25\ [2(G_p/\omega)_{max}/(q.A)] \qquad (2.8)$$

$$\tau = 1.98/\omega$$

The nature of the admittance characteristics are to a large extent affected by the statistical fluctuations in the interface potential. This fluctuation in the potential is due to random

distribution of charges in the oxide, ionized impurities in silicon and non uniform oxide thickness. To take this into account a statistical model was proposed by Nicollian and Goitzberger [9] which is described below.

The plane of the device is conceptually divided into a number of squares of equal area called the characteristic area such that the interface potential is uniform over this area. The admittance of the continuum is regarded as due to the states within a characteristic area. The total admittance is then obtained by integrating the contribution from each characteristic area over all the characteristic areas of the device.

The equivalent circuit of the device therefore becomes as shown in the Fig. 2.4. The interface state branch of the equivalent circuit now consists of a number of series RC circuits each corresponding to a characteristic area and all such series RC branches are connected in parallel to give the total contribution towards the interface state admittance.

The conductance in this case also goes through a peak when $\omega\tau = 2.5$ and the peak value is proportional to the interface state density and the proportionality factor is a function of interface potential.

The behaviour of the device with interface potential statistical fluctuations is governed by the following relations assuming a Gaussian distribution. Equivalent parallel capacitance and conductance are given by [9],

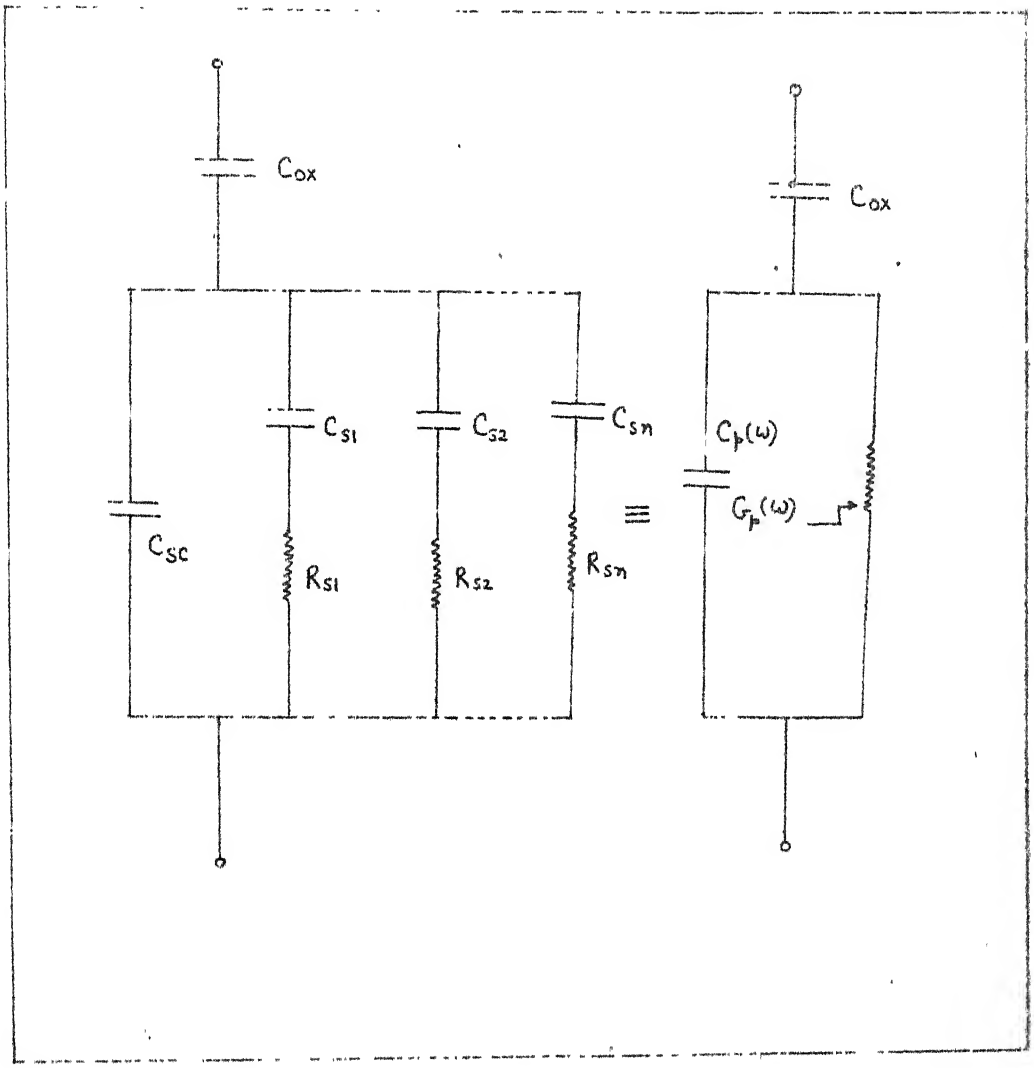

Fig. 2.4: Equivalent Circuit Taking into Account the Statistical Fluctuation in the Interface Potential.

$$(a)\quad C_p = C_{sc} + q\,A\,N_{ss}\,[2\pi\,(\sigma_s^2 + \sigma_B^2 + \sigma_x^2)]^{-1/2} \int_{-\infty}^{\infty} \exp.\,[-(z+y)]\,\tan^{-1}\,(e^y)\,d\,U_s$$

$$(b)\quad G_p = \frac{q\,A\,N_{ss}}{2}\,[2\pi\,(\sigma_s^2 + \sigma_B^2 + \sigma_x^2)]^{-1/2} \int_{-\infty}^{\infty} \exp.[-(z+y)]\,\ln\,[1+\exp\,(2y)]\,d\,U_s \qquad (2.9)$$

where, $y = \ln\,(\omega\tau)$

$$z = [U_s - \ddot{U}_s]^2/2(\sigma_s^2 + \sigma_B^2 + \sigma_x^2)$$

$$\ddot{U}_s = q\,\phi_i/kT$$

and $U_B = q\,\phi_B/kT$

σ_s, σ_B and σ_x are the standard deviations of surface potential, bulk charge and oxide thickness respectively of the distribution and are given by the relations given below [9].

$$(a)\quad \sigma_s = \frac{W\,(qQ/\alpha)^{1/2}}{V_T[\varepsilon_s + W.C_{ox}]}$$

$$(b)\quad \sigma_B = \frac{q\,(N_A.W)^{1/2}\,[1-\exp.(-\ddot{U}_s)]}{2\,V_T\,[\varepsilon_s + W.C_{ox}]}\,,\quad \text{for p-Si}$$

$$(c)\quad \sigma_x = \frac{q\,N_A\,W^2[1-\exp(-\ddot{U}_s)]}{V_T\,\varepsilon_{ox}\,[A/C_{ox} + A/C_{sc}]}\,,\quad \text{for p-Si} \qquad (2.10)$$

(d) $W = \varepsilon_s / C_{sc}$

(e) $\alpha = 1.5\ W$

(f) $Q = (C_{ox}/A)\ [-V + \phi_i] - Q_{sc}$

Therefore, the interface state density and time constant are given by the relation

$$N_{is} = (1/c)\ [2\ (G_p/\omega)_{max}/(q.A)]$$

$$\tau = 2.5/\omega \qquad (2.11)$$

where c is the proportionality constant and is a function of interface potential.

To determine the energy location and the capture cross section the nature of the charge exchange should be understood first.

In dark the charge exchange can take place only between the interface states and the majority carrier band but under illumination charge exchange can take place either between the conduction band and the interface states at the electron imref or between the valence band and the interface states at the hole imref. The former will prevail if $\sigma_e n_s > \sigma_h . p_s$ otherwise the latter [1]. But as σ_e and σ_h are to be determined by the conductance method itself some alternative method should be there to identify the charge exchange. In the method given below it is assumed that the capture cross section is independent of energy. Hole or electron peak identification is done with

the help of G_p/ω vs. frequency curves plotted at different biases [1].

$(G_p/\omega)_{max}$ would move towards smaller frequencies with more negative values of bias if electron exchange with the conduction band were to be the dominant one and shifting towards higher frequencies with more negative values of bias implies that the dominant process is exchange of holes with the valence band.

After ascertaining whether hole exchange or the electron exchange is the dominant process the capture cross section can be calculated from the following equations [9]

$$\sigma_e = \frac{1}{v \tau n_s} \qquad \text{for electron exchange}$$

$$\sigma_h = \frac{1}{v \tau p_s} \qquad \text{for hole exchange}$$

where v is the thermal velocity and p_s and n_s are the hole and electron densities respectively at the surface and τ is the time constant corresponding to the frequency at which $(G_p/\omega)_{max}$ occured.

Energy locations of the states can be obtained using equations (2.6).

REFERENCES

1. S. Kar and S. Varma, to be published.

2. T. Sakurai and T. Sugano, J. Appl. Phys. 52(4), April 1981, pp. 2889-2896.

3. P.J. Caplan, E.H. Pointdexter, B.E. Deal and R.R. Razouk, J. Appl. Phys., 52, 879 (1981).

4. E.H. Pointdexter, G.J. Gerardi, M.E. Rueckel, P.J. Caplan, N.M. Johnson and D.K. Biegelson, J. Appl. Phys., 56, 2844 (1984).

5. R.A. Gdula, IEEE Transactions on Electron Devices, Vol. ED 26, No. 4, April 1979, pp. 644-647.

6. L.N. Terman, Solid State Electronics, 5, 285 (1962).

7. C.N. Berglund, IEEE Trans. on Electron Devices ED-13, 701 (1966).

8. M. Kuhn, Solid State Electronics, 13, 873 (1970).

9. E.H. Nicollian and A. Goetzberger, Bell Syst. Tech. Journal, 46, 1055 (1967).

10. T.C. Poon and H.C. Card, J. Appl. Phys., 51, 5880 (1980).

11. T.C. Poon and H.C. Card, J. Appl. Phys., 51, 6273 (1980).

12. S. Kar and S. Varma, J. Appl. Phys., 54, 1988 (1983).

13. S. Kar, S. Varma, P. Saraswat, and S. Ashok, J. Appl. Phys., 53, 7039 (1982).

14. S.M. Sze, Physics of Semiconductor Devices, (Wiley, New York, 1983).

CHAPTER III

FABRICATION AND MEASUREMENT

3.1 Sample Fabrication

The starting materials were p type epitaxial Silicon wafers with (100) surface orientation. The layer resistivity was 1 Ohm-cm. Class 100 clean environment was maintained through out the fabrication process.

The wafers were initially degreased in warm trichloroethylene, degreased in warm acetone, cleaned ultrasonically in acetone and finally degreased in warm methanol. After degreasing they were etched in HF, rinsed in deionized water of resistivity about 14-16 M Ohm-cm and dried in dry filtered nitrogen gas. Subsequently preoxidation was carried out in a Thermco resistance heated furnace in dry oxygen at 1100°C for 30 minutes at atmospheric pressure. The wafers were then etched in HF, rinsed in deionized water and then dried in dry nitrogen. Final oxidation was carried out in dry oxygen at 1100°C at atmospheric pressure for 30 minutes. No post oxidation annealing was carried out.

The wafers were introduced into the vacuum chamber of a Varian VT-112B ultra high vacuum system immediately after the

oxidation was complete. The UHV system used had sorption, sublimation and sputter ion pumps. After the oxidized wafers were introduced into the vacuum chamber it was pumped down to 1.0×10^{-7} torr, substrate temperature was brought upto 300°C. Filtered dry oxygen was then introduced and the partial pressure of oxygen was adjusted to 1.0×10^{-5} torr. Layers of tin doped indium oxide were deposited on the substrate by upward E-Beam evaporation of tin containing (10.0 atomic percent) indium oxide tablets. Initially, the substrates were protected from outgassing of the indium oxide tablet by a shutter arrangement.

3.2 Evaporation Set Up

As mentioned earlier the evaporation of tin doped indium oxide was carried over in the Varian Model 112B ultra high vacuum system with 12 inch diameter belljar.

The system employs two liquid nitrogen cooled sorption pumps as the roughing pumps to evacuate the chamber from atmospheric pressure to about 1×10^{-3} torr. The two sorption pumps are employed in tandem. The first sorption pump is used to pump down the chamber to about 1-2 torr which is then sealed off and the other sorption pump activated to achieve a pressure of about 1 m torr. The system is evacuated further with the help of sputter ion pumps which in conjunction with sublimation pump fitted in the system can bring down the system pressure to about 2×10^{-11} torr, if stainless steel chamber is used and adequate baking carried out. With a glass belljar, pressure upto about

2×10^{-9} torr could be obtained, though pressure upto about 1×10^{-7} torr could be obtained easily in a reasonably short time (approx. 40 min.).

To measure the pressure from 1.0 torr to 1.0×10^{-3} torr thermocouple gauge is used while dual filament ionization gauge reads chamber pressure from 10^{-4} torr to 2×10^{-11} torr.

The triode ion pumps or the sputter ion pumps can give the pressure of the system in the pump region as the current in the pump depends upon the pressure. A pressure interlock is provided in the ion pump control unit which switches off the pump if pressure exceeds 1×10^{-5} torr.

Evaporation was carried out using a Varian 2 kW, 3-crucible electron gun with stainless steel crucibles, cooled by chilled recirculating water. Substrates were located about 17 cm above the tablet and were supported on molybedenum shadow masks in a substrate holder. Similarly back Au contact was formed of filament evaporation in a separate Varian VT-112A UHV system after the oxide from the back of the wafer was dissolved in HF while the front protected by apiezon wax. No post-metallization annealing was carried out.

3.3 Measurement

Out present work required the measurement of capacitance and conductance of the devices at various frequencies and biases under a varying intensity of illumination. The measurements at

low frequencies (60 Hz and 120 Hz) were made on General Radio 1621 precision capacitance measurement system which can give both capacitance and conductance while high frequency measurement were made on HP 4192 digital Impedance analyzer which is a very powerful equipment for impedance measurements of a device at different biases and frequencies over a wide range. Provisions for sweep bias and sweep frequency helps in quick measurements.

3.3.1 Low Frequency Measurements

Capacitance, conductance vs. voltage measurements for the device in dark as well as under illumination at 60 Hz and 120 Hz were made using a General Radio 1621 capacitance measurement system, a Keithley 616 digital electrometer and a finely adjustable d.c. power supply.

All measurements were carried out at room temperature with the samples placed in a electrically shielded box. Contact to the front gate of the device was established through a gold plated sharp pointed telescopic spring probe mounted on a micromanipulator while the contact to the back contact was made with the help of a copper block over which the sample was placed.

Tungston lamp illumination was used for measurements under optical illumination and the light was allowed into the box onto the sample through a tiny slit. The area of the

front gate was calculated from the diameter measured with a Unitron optical microscope.

3.3.2 High Frequency Measurements

Generally, any mutual inductance, interference of the measurement signals and unwanted residual factors in the connection method which are incidental to ordinary terminal measurement methods significantly affect the measurement at higher frequencies.

To avoid these problems four terminal pair configuration measurements were carried out with the help of HP 4192 digital impedance analyser.

To minimize the effect of lead capacitance and inductance at higher frequencies the internal connection leads of the sample box which connect the spring probe and the copper block to the external BNC terminals were made as short as possible.

3.3.3 Principle of Four Terminal Pair Configuration Measurements

In this configuration the unknown terminals consist of four connectors: High Current (HCUR), High Potential (HPOT), Low Potential (LPOT) and Low Current (LCUR) as shown in Fig. 3.1. To avoid interference of measurement signals current terminals are separated from potential terminals. The purpose of the current terminals is to cause a measurement signal current to flow through the sample and the potential terminals detect the

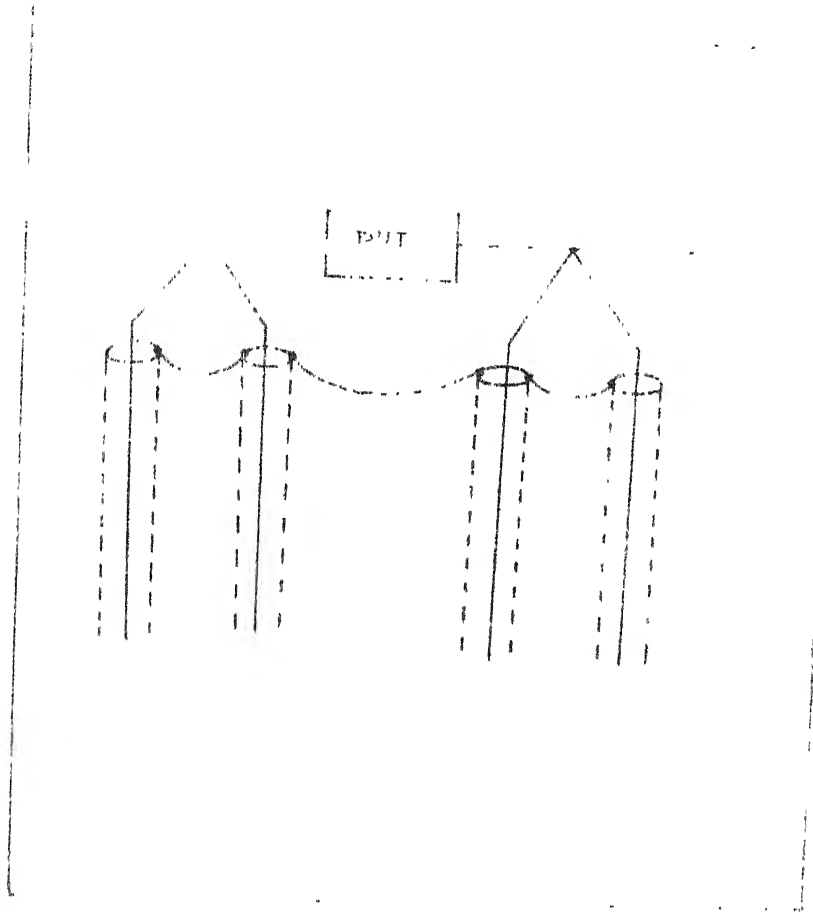

Fig. 3.1: Four terminal [illegible] configuration.

voltage drop across the DUT [1]. The distinctive feature of the four terminal pair configuration is that the outer shield conductor works as the return path for the measurement signal current. The same current flows through both the centre conductors and the outer shield conductors in opposite directions cancelling the magnetic fields produced by each other as shown in Fig. 3.2. Since the measurement signal current does not develop an inductive magnetic field, the test leads do not contribute additional measurement errors due to self or mutual inductance between the individual leads. Thus the four terminal pair method combines the advantages of the four terminal method in low impedance measurements while providing the shielding required for high impedance measurements.

REFERENCE

1. H.P. 4192, Digital Impedance Analyser Manual.

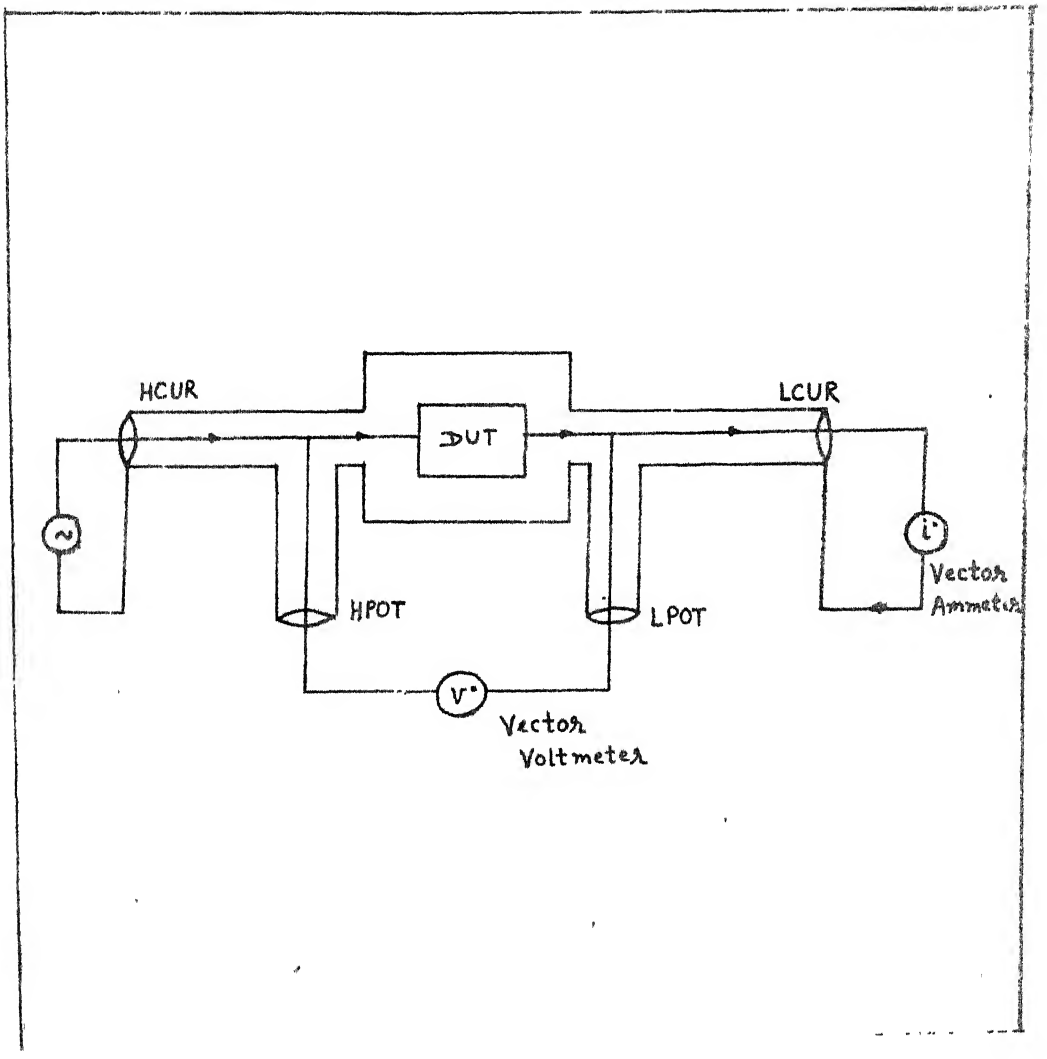

Fig. 3.2: Principal of Four Terminal Pair Configuration Measurement.

CHAPTER IV

ANALYSIS RESULTS AND DISCUSSION

4.1 Capacitance Data Analysis

4.1.1 Analysis in Dark

Capacitance data analysis is based on the low frequency capacitance technique. To extract interface state capacitance out of the total admittance of the device which as mentioned in 2.2.1 consists of the space charge capacitance C_{scd}, oxide capacitance C_{ox} and the interface capacitance C_{is}, C_{scd} and C_{ox} should be known.

The space charge layer capacitance C_{scd} is given by the relation

$$\frac{C_{scd}}{A} = \frac{dQ_{scd}}{d\phi_i} \qquad (4.1)$$

where Q_{scd} is the charge in the space charge layer per unit area and ϕ_i is the interface potential.

Q_{scd} is given by the following relation [1] for the p-type silicon substrate.

(a) $$Q_{scd} = \mp \frac{2\varepsilon_s kT}{q.L_D} \cdot F(U_s, n_{po}/p_{po})$$

where,

$$\text{(b)} \quad F(U_s, n_{po}/p_{po}) = [(\exp U_s - U_s - 1) + (p_{no}/n_{no})(\exp(-U_s) + U_s - 1$$

$$\text{(c)} \quad L_D = [2\varepsilon_s \, kT/(q^2 \, p_{po})]^{1/2} \qquad (4.2)$$

$$\text{(d)} \quad p_{po} = N_A, \; p_{po} \, n_{po} = n_i^2$$

$$\text{(e)} \quad U_s = q \, \phi_i / kT$$

From equations (4.1) and (4.2) expression for C_{scd} can be derived in terms of ϕ_i and other parameters which has already been presented in Chapter II equation (2.1).

The oxide capacitance C_{ox} is due to a plane parallel capacitor and it can be determined if oxide thickness is known but as we know that the dielectric permittivity of thin thermal oxides is not known accurately it is not advisable to compute the value of C_{ox} using this procedure. Instead the value of C_{ox} was estimated from the saturation capacitance in strong inversion and accumulation. Due to various practical constraint the MOS capacitance never saturates to the C_{ox} value but always to a value lower than it but for the calculation of minimum value of space charge capacitance in dark and subsequently doping density it serves the purpose and more accurate value of C_{ox} can be determined by a different procedure which is explaine in a later portion of the chapter.

The C-V characteristics of the device are shown in the Fig. 4.1 for dark and illumination conditions. The doping densi

is calculated by a few iterations using the following equations (4.3) [1]

$$\text{(a)} \quad N_{doping} = 2(C_{scd}^{min}/A)^2 \, \phi_i^{invd} / q\varepsilon_s$$

$$\text{(b)} \quad C_{scd}^{min} = [(1/C_{hfd}^{min}) - (1/C_{ox})]^{-1} \qquad (4.3)$$

$$\text{where} \quad \phi_i^{invd} = V_G - 2\phi_p \quad \text{for} \quad p - Si$$

$$\text{and} \quad \phi_p = (kT/q) \ln (N_V/N_A)$$

The value of C_{hfd}^{min} is the minimum capacitance in strong inversion at the highest frequency and is read from the C-V curves of Fig. 4.1.

After the doping density has been estimated by iterations the value of C_{scd} is computed at various values of interface potential Φ_i using equations (2.1) and plotted semilogarithmically as a function of interface potential Φ_i as shown in the Fig. 4.2.

To obtain the inter-relationship between the applied bias V and the voltage appearing across the interface Φ_i, graphical integration is done of the low frequency capacitance - voltage curve based on the following relation [2]

$$\phi_i(V_1) - \phi_i(V_2) = \int_{V_1}^{V_2} [1-(C_{lfd}/C_{ox})] \, dV + K \qquad (4.4)$$

where K is a constant.

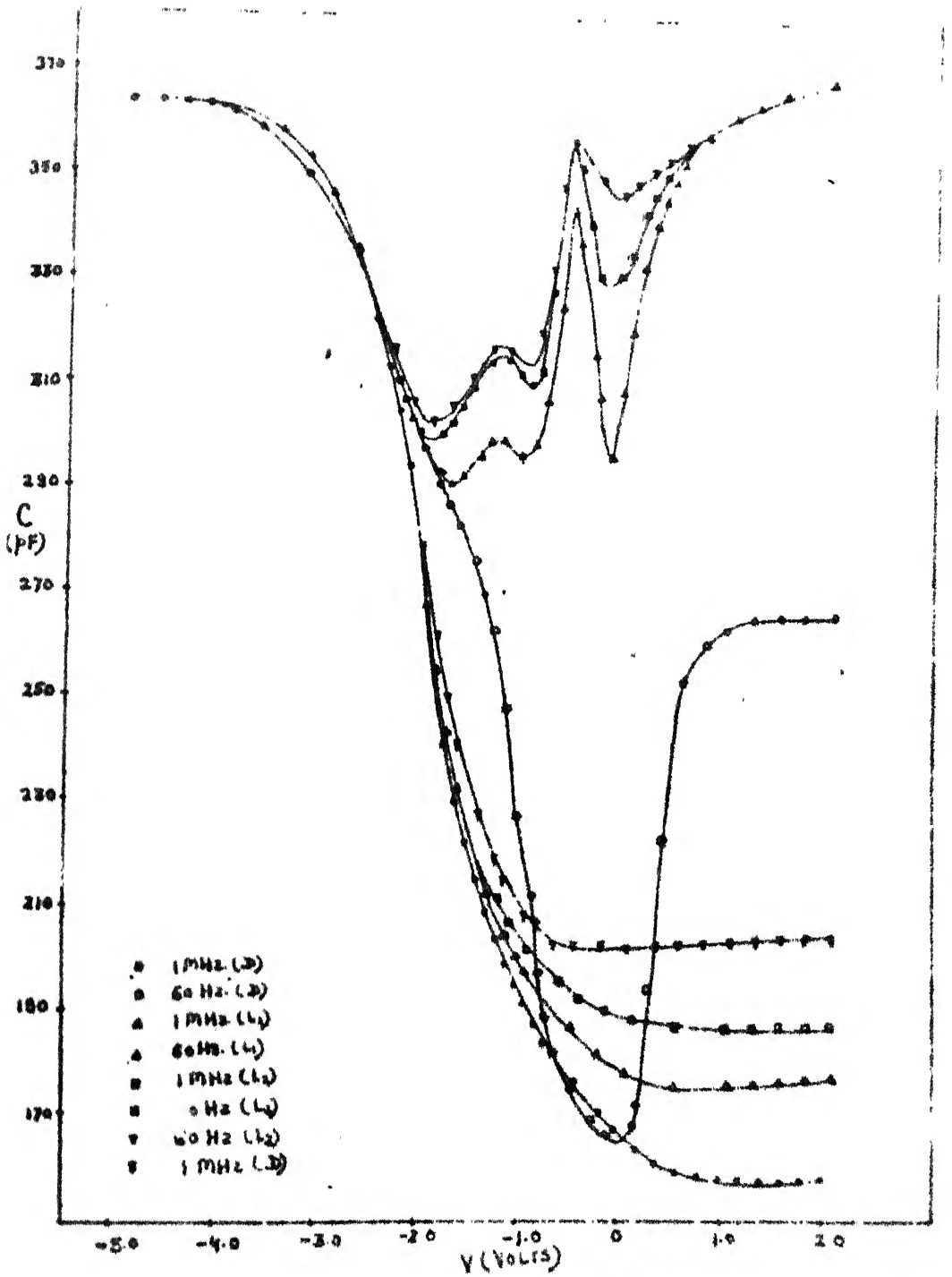

Fig. 4.1: Capacitance-Voltage Curves of the structure a 60 Hz and 1 MHz in dark and under illumination levels L_1, L_2 and L_3.

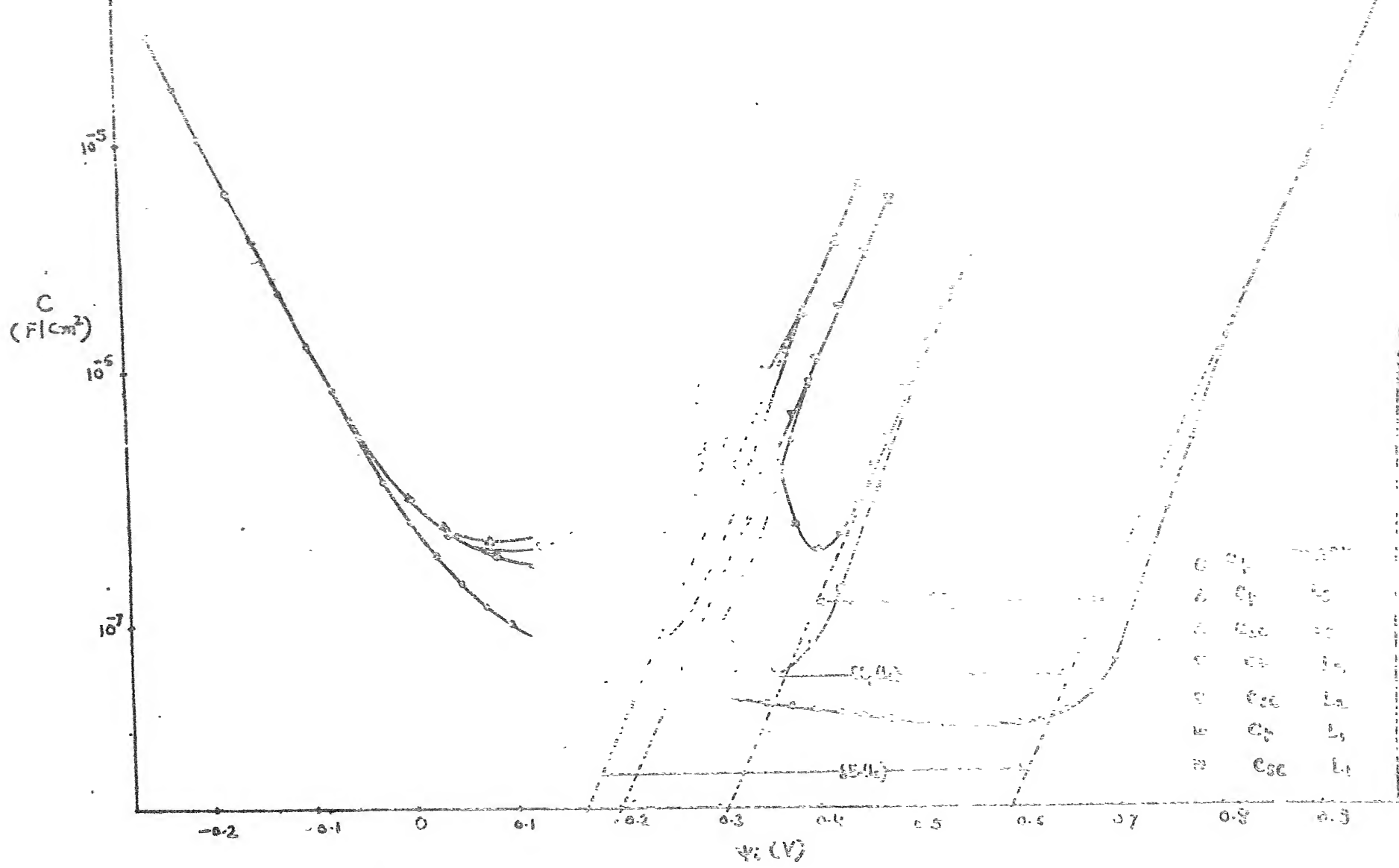

Fig. 4.2: Plots of the space charge capacitance and the equivalent parallel capacitance in dark and under illumination intensities of L_1, L_2 and L_3.

Since the value of C_{ox} obtained previously is not exact, to accurately determine it a few iterations as described below are required.

The measured low frequency dark MOS capacitance is reduced to the parallel capacitance by the following relation [3]

$$1/C^{p}_{lfd} = [1/C_{lfd}(V)] - [1/C_{ox}] \qquad (4.5)$$

Initially the graphical integration is carried out in the accumulation region only and the values of C^{p}_{lfd} calculated from (4.5) are tried to match with C_{scd} obtained theoretically, the two should be same as in strong accumulation the capacitance is mainly due to space charge capacitance. If the matching is not proper the value of C_{ox} should be changed and the above procedure repeated till the two match with each other.

Once the linear part of the experimental ln C^{p}_{lfd} vs. ϕ_i curve is fitted with ln C_{scd} vs. ϕ_i curve the value of constant K can be obtained.

Once the oxide capacitance has been optimized the value of C^{p}_{lfd} (ϕ_i) is calculated over the entire range of bias from strong accumulation to strong inversion and ln C^{p}_{lfd} vs. ϕ_i is plotted on the same graph as C_{scd} (ϕ_i).

The interface state density is then obtained from the difference between C^{p}_{lfd} and C_{scd} as per the relation given below [3],

$$N_{is} = \frac{C_{is}}{q} = \frac{C^{p}_{lfd} - C_{scd}}{q} \qquad (4.6)$$

The energy location corresponding to an interface potential, in the band gap is [3]

$$E - E_V = q\,(\phi_p + \phi_i) \quad p - Si \qquad (4.7)$$

ϕ_i vs. V and N_{is} vs. $E-E_V$ can be plotted now.

4.1.2 Data Analysis Under Illumination

The analysis under illumination differs slightly from that in dark because of the fact that under the illumination due to photogeneration of electron-hole pairs the minority carrier Fermi level is no longer the same as the majority carrier Fermi level but moves towards the minority carrier band edge as the illumination is increased. Consequently there are two quasi Fermi levels in the band gap one due to electrons E_F^e and the other due to holes E_F^h separated by quasi Fermi level separation ΔE_F.

Due to this shifting of minority carrier Fermi level towards the minority carrier band edge the amount of band binding required to achieve weak inversion and strong inversion reduces by an amount equal to the Fermi level separation and this leads to a change in space charge capacitance in inversion when illumination is employed.

Under illumination the space charge capacitance is calculated from the values of doping density and the experimentally

determined value of quasi Fermi level separation using the relations [4]:

$$C_{scl} = (\varepsilon_s/L_D)[1-\exp(-U_s) + (n'_{po}/p'_{po})(\exp(U_s)-1)]/$$

$$F(U_s, n'_{po}/p'_{po}, \quad p - Si \qquad (4.8)$$

where,

$$p'_{po} = p_{po} = N_A$$

$$n'_{po} = n_{po} \exp(\Delta E_F/kT)$$

As can be seen from the above equation the value of C_{scl} is the same as C_{scd} except in the region of inversion and so it is sufficient, if we calculate C_{scl} in the inversion region.

The low frequency parallel capacitance under illumination is obtained by the following equation [3]

$$1/C^p_{lfl} = 1/C_{lfl} - 1/C_{ox} \qquad (4.9)$$

The interface potential as a function of bias is obtained by the integration of the corresponding low frequency curve under illumination by the same procedure as was used in dark. The ϕ_i vs. V plot is shown in Fig. 4.3.

The quasi Fermi level separation can be obtained by three different methods.

The first method is based on the fact that under the illumination the onset of strong inversion takes place at a value of interface potential which is smaller than the corresponding value in dark by an amount equal to the imref separation.

Fig. 4.3 [illegible] potential vs. [illegible]
in dark and under illumination for
I_1, I_2 and I_3.

This interface potential ϕ_i^{invl} can be obtained from the measured high frequency MOS capacitance minimum under illumination using the following relation [4]

$$\phi_i^{invl} = [q\ \varepsilon_s\ N_{doping}]/2\ (C_{scl}^{min}/A)^2 \qquad (4.10)$$

where,

$$C_{scl}^{min} = [1/C_{hfl}^{min} - 1/C_{ox}]^{-1}$$

and the value of ΔE_F can be found out by the difference

$$\Delta E_f = q|\phi_i^{invd} - \phi_i^{invl}|$$

The high frequency minimum value of capacitance used here should be at the highest frequency possible which in our cas is 1 MHz. The difference in 1 MHz and 100 KHz minimum capacitanc value in strong inversion was noticed and obviously if 100 KHz curve is used the value of ΔE_f so obtained will not be accurate.

The second method to determine ΔE_F is based on the fact that if we integrate the low frequency curve under illumination from accumulation to inversion region and sum up all the ϕ_i so obtained the sum will be equal to $E_G - \Delta E_F$ as while integration the interface potential scans whole of the band gap except the region between the two quasi Fermi levels.

Thus we have [3]

$$\Delta E_F = E_g - q\ \Sigma\ \phi_i \qquad (4.11$$

where $\Sigma\ \phi_i = \int_{acc}^{inv} [1 - C_{lfl}/C_{ox}]\ dV$

The source of error in this method is the fact that it is not possible to go into strong accumulation and strong inversion regions.

The third method which is the one employed in our work is based on the parallel shift in strong inversion between the theoretical ln C_{scd} vs ϕ_i characteristics and the experimental ln C^l_{lfl} curve. In strong inversion the simplified expression for C_{scl} is [3]

$$C_{scl} = (\varepsilon_s/L_D) \exp [(q\phi_i + \Delta E_F)/2kT], \text{ p-Si}$$
$$\simeq C_{scd} \exp [\Delta E_F/2kT] \qquad (4.12)$$

If C_{is} is quite small as compared to C_{sc} then the graph of ln C^p_{lfl} vs. ϕ_i would be a straight line and the parallel shift of this line from the dark C_{sc} curve would be equal to ΔE_F as shown in the Fig. 4.2.

When the ln C^p_{lfl} vs. ϕ_i curve is plotted completely and from the value of ΔE_f thus obtained C_{scl} calculated from equation (4.8) plotted, the value of C_{is} can be determined from the difference and value of N_{is} found out by [3]

$$N_{is} = (C^p_{lfl} - C_{scl})/q \qquad (4.13$$

As mentioned earlier in theory the state occupancy is controlled by electron imref or hole imref depending upon whether at the interface $(E_c - E^e_F)$ is smaller or, $(E^h_F - E_v)$.

This can be put in one condition as below [3].

For p-Si if

$$[V_G - (\phi_i + \phi_p + \Delta E_f/q)] < (\phi_i + \phi_p)$$

is satisfied electron imref will control state occupancy otherwise hole imref. But in the above method it has been assumed the hole and electron capture cross sections are same and they are independent of energy.

If the above condition is not true then $n_s \sigma_e >> p_s \sigma_h$ criterion will have to be applied.

If the capture cross section is not dependent upon energy then the condition becomes [3]

$$[V_G - (\phi_i + \phi_p - \Delta E_f/q)] < [\phi_i + \phi_p - (kT/q) \ln (\sigma_h/\sigma_i)]$$

After identifying the dominant imref energy location is determined from equations (2.6) and the interface state density profile plotted.

4.2 Conductance Data Analysis

In this method information regarding the interface states is obtained by making use of the equivalent parallel conductance data.

The equivalent parallel conductance G_p and the equivalent parallel capacitance C_p are obtained from the measured capacitance C_m and conductance G_m using the following equations [5]

$$G_p/\omega = \frac{\omega C_{ox}^2 \, G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$

$$C_p = \frac{C_{ox} [\omega^2 C_m (C_{ox} - C_m) - G_m^2]}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad (4.14)$$

In our present work, for conductance data measurement were taken to obtain C_m, G_m vs. frequency data taking bias across the device as the parameter. One of the advantage of obtaining C_m, G_m vs. frequency data instead of C_m, G_m vs. bias is that the identification of the source of the peaks in the G_p/ω vs. frequency curves becomes direct as no separate plots are to be prepared to determine it.

The G/f vs. frequency and G_p/ω vs. frequency plots under illumination are shown in the Figs. 4.4 to 4.7 respectively.

As mentioned in the theory in section 2.2.2 the G_p/ω vs. frequency curves will go through a maxima as shown in the Fig. 4.4-7 . All these peaks at various biases will be located at such a frequency that $\omega\tau = 1$, 1.98, or 2.5 depending upon whether the interface state under consideration is a single level, continuum or continuum under statistical fluctuations of interface potential respectively.

The identification of the model of the interface state is done by comparing the half widths of G_p/ω vs. frequency curves at various biases with that of the G_p/ω vs. $\omega\tau$ characteristics

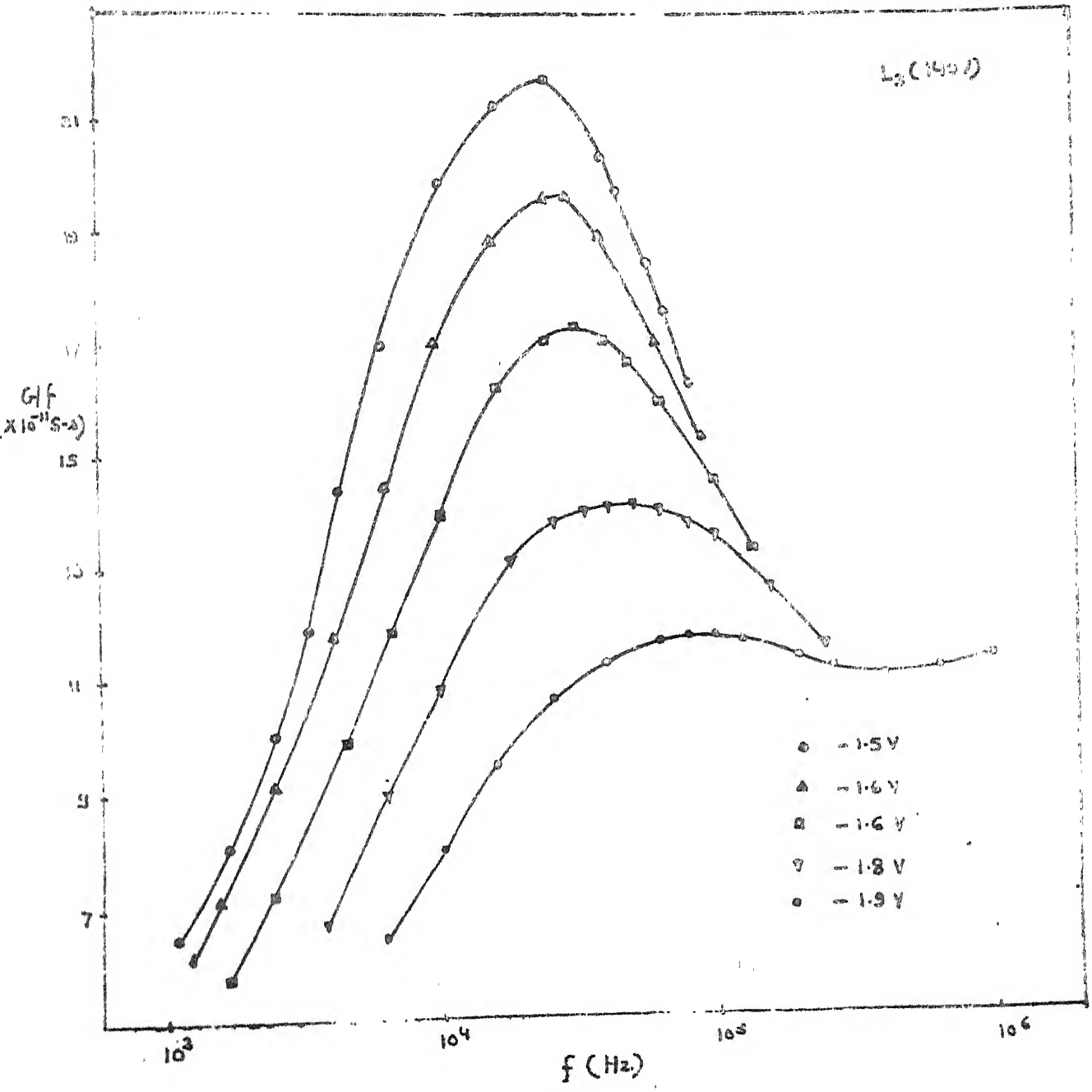

Fig. 4.4: G/f vs. f plot for majority carrier peaks under illumination level L_3.

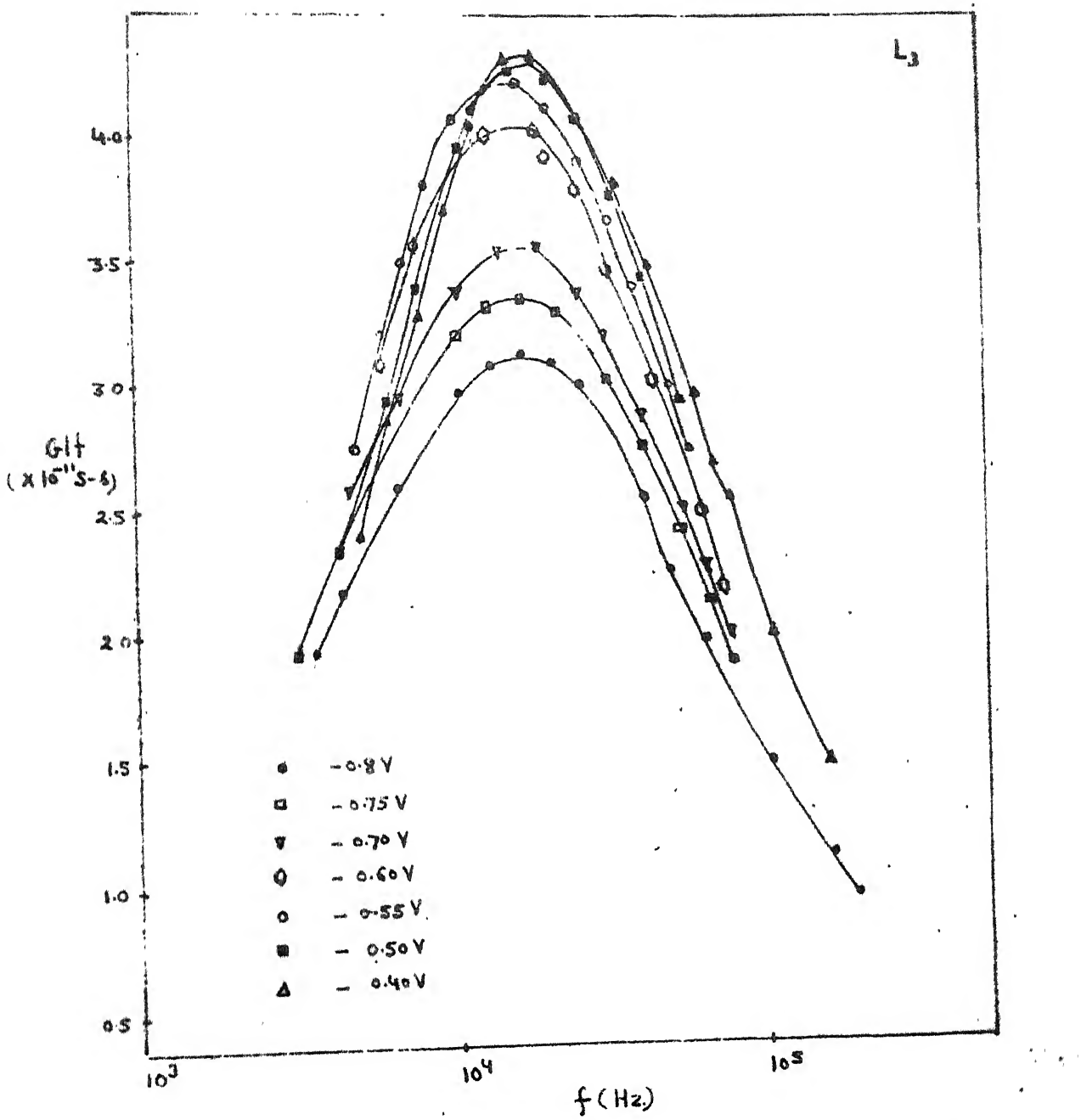

Fig. 4.6: G/f vs. f plot for minotiry carrier peaks under illumination level L_3.

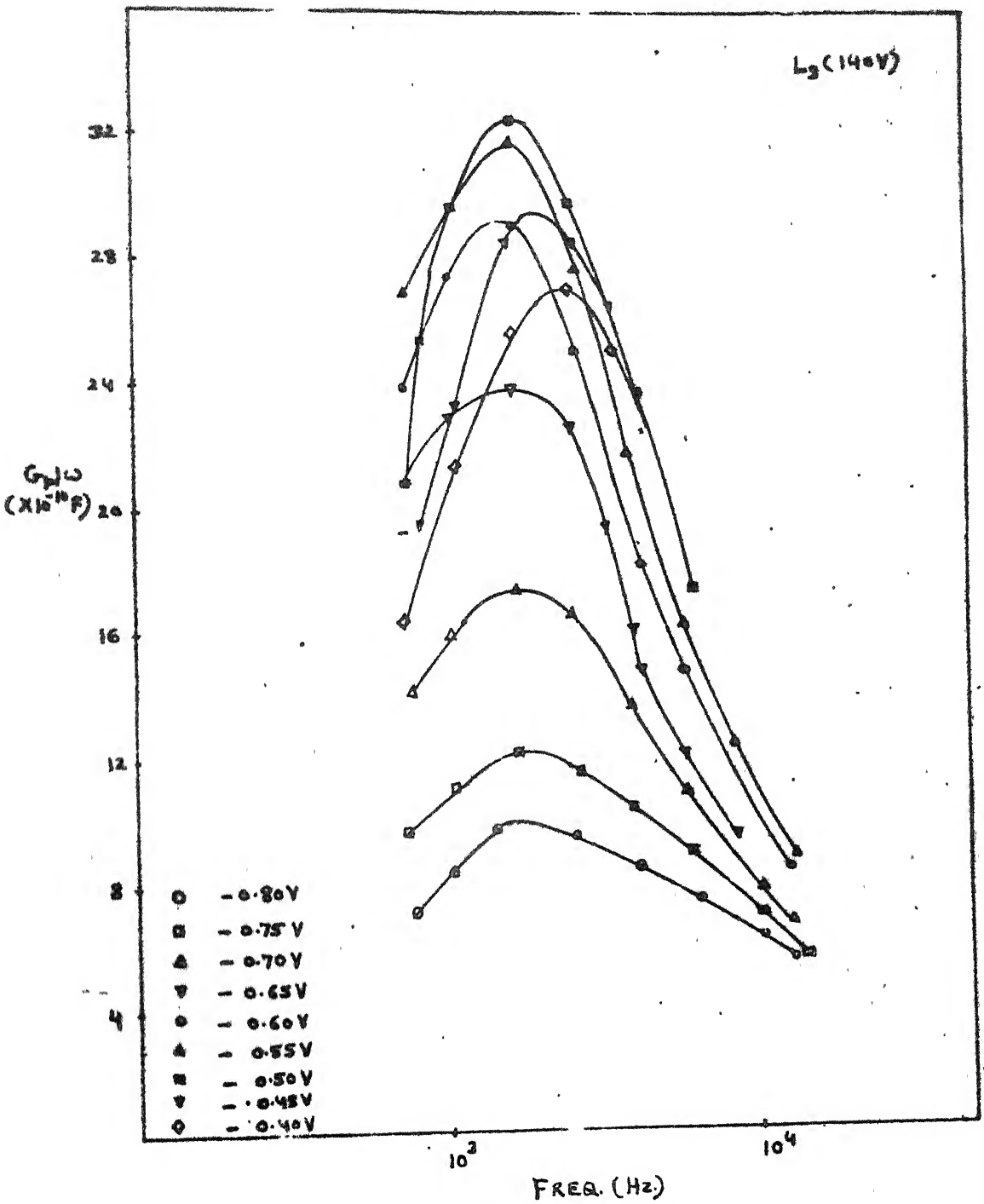

Fig. .7: G_p/ω vs. f plot for minority carrier peaks under illumination level L_3.

calculated by Nicollian and Goetzberger [5] for the three cases of single level, continuum of states and state continuum under the influence of statistical fluctuations in surface potential.

Identification of the peak whether it is due to electrons on holes is done by observing the nature of the shift in the peaks of the curve as the bias is changed and it is explained in Chapter II under the section 2.2.2.

The interface state density and the time constant corresponding to these peaks for the three different cases are given by the expressions given below [5]

Single Level

$$N_{is} = 2\,(G_p/\omega)_{max}/(q.A)$$
$$T = 1/\omega \qquad (4.15)$$

Continuum of States

$$N_{is} = 1.25\,[2(G_p/\omega)_{max}/(q.A)]$$
$$= 1.98/\omega \qquad (4.16)$$

Continuum with Statistical Fluctuations in ψ_s

$$N_{is} = (1/c)\,[2(G_p/\omega)_{max}/(q.A)]$$
$$= 2.5/\omega \qquad (4.17)$$

Next, to determine the capture cross section for holes and electrons the values of carrier densities at the interface have to be known. These surface concentrations for holes p_s and

electrons n_s can be calculated if surface potential is known. Surface potential corresponding to a certain bias can be determined using the graph of Fig. 4.3.

The equations giving capture cross sections in terms of surface concentration of carriers, mean thermal velocity of carriers $\bar{v}$ and the time constant τ are reproduced below [5]

$$\sigma_h = \frac{1}{\bar{v}\,\tau\,p_s} \qquad \text{for holes}$$

$$\sigma_e = \frac{1}{\bar{v}\,\tau\,n_s} \qquad \text{for electrons} \qquad (4.18)$$

4.3 Results and Discussion

As mentioned in the previous sections the p-type $Si/SiO_2/In_2O_3$ structure, the top In_2O_3 transparent gate of which was deposited with E-Beam Evaporation was investigated employing both the capacitance and conductance techniques under illumination and the effects of radiation damage identified in the interface state density profile.

As can be seen from the capacitance voltage characteristics of the device 60 Hz was chosen as the low frequency for our C-V analysis and this is justified because of the fact that at the lowest illumination level there was not any dispersion observed between the 60 Hz and 120 Hz characteristics moreover the 60 Hz characteristics under illumination saturates in accumulation as well as in strong inversion region showing that under illumination

the inversion layer is completely able to follow the 60 Hz signal because of enough number of minority carriers being available due to photo generation under illumination.

Similarly the 60 Hz dark capacitance voltage characteristics shows that in dark the inversion layer is not completely able to follow the 60 Hz signal and consequently the device capacitance in strong inversion region is quite low but the interface states are able to follow the 60 Hz signal which is clearly seen as the kink in the 60 Hz curve.

The two sets of peaks in the low frequency capacitance voltage characteristics under illumination were seen to give rise to interface state density peaks near the valence band and the conduction band edges.

Selecting the high frequency for C-V analysis is quite important as the accuracy in the determination of doping density N_A is affected by it. If it is not high enough then the high frequency minimum obtained in strong inversion may not be the true minimum due to some contribution from either the interface states or, due to a very small response from inversion layer thus contributing some capacitance. In our work we noticed the difference between the minimum capacitance of 100 KHz and 1 MHz curves in strong inversion. But increasing the frequency to higher values is also not advisable due to practical constraints in high frequency measurement as explained in Chapter II. 1 MHz was chosen

as the high frequency in our work and its suitability was ascertained by calculating the parallel capacitance C_p in dark corresponding to the capacitances measured at various biases at 1 MHz and it was plotted on a semi-logarithmic graph sheet against the interface potential. The theoretical space charge capacitance C_{sc} was also plotted on the same sheet against interface potential. The two curves matched quite well as shown in the Fig. 4.8 establishing the suitability of 1 MHz frequency and also it worked as a check on doping density computation.

Quasi Fermi level separation was determined under the various illumination intensities employing all the three methods discussed in the theory. The method which makes use of the shift in the C_{sc} curve in strong inversion and the one which determines the separation by making use of minimum high frequency capacitance in strong inversion seems to give the value of imref separation right at the interface as both these methods make use of the capacitance in strong inversion which has got a very dominant contribution from the inversion layer which extends to only a few Amstrongs inwards from the interface thus the quasi Fermi level separation so obtained presents the required parameter right at the interface.

The quasi Fermi level separation for various illuminations obtained by these two methods in our work agreed quite well with each other.

The third method to determine the quasi Fermi level separation i.e. the method of integration does not give the value at the interface but some sort of weighted average along the space charge layer as the capacitance is integrated from accumulation to inversion to obtain the separation.

The Fermi level separation found by this method was higher than that obtained by the first two methods. This can be attributed to the fact that the method will give the exact value of Fermi level separation if the curve is integrated from the point in strong accumulation where the valence band (for p-type sample) just touches the quasi Fermi level for holes at the interface to a point in strong inversion where the conduction band just touches the quasi Fermi level for electrons at the interface. But in practice we never go to such deep accumulation and inversion and consequently while integrating instead of tracing ($E_g - \Delta E_F$) of the band gap we scan a lower value which gives rise to a higher value of Fermi level separation.

The interface state density profile obtained by capacitance method is shown in the Figure 4.9 for various illumination conditions as well as for dark.

In dark interface state profile can be obtained only in lower band gap half (for p - type Si) as the states in the upper band gap half cannot respond to the signal. Under the application of a uniform background of illumination two peaks are obtained in

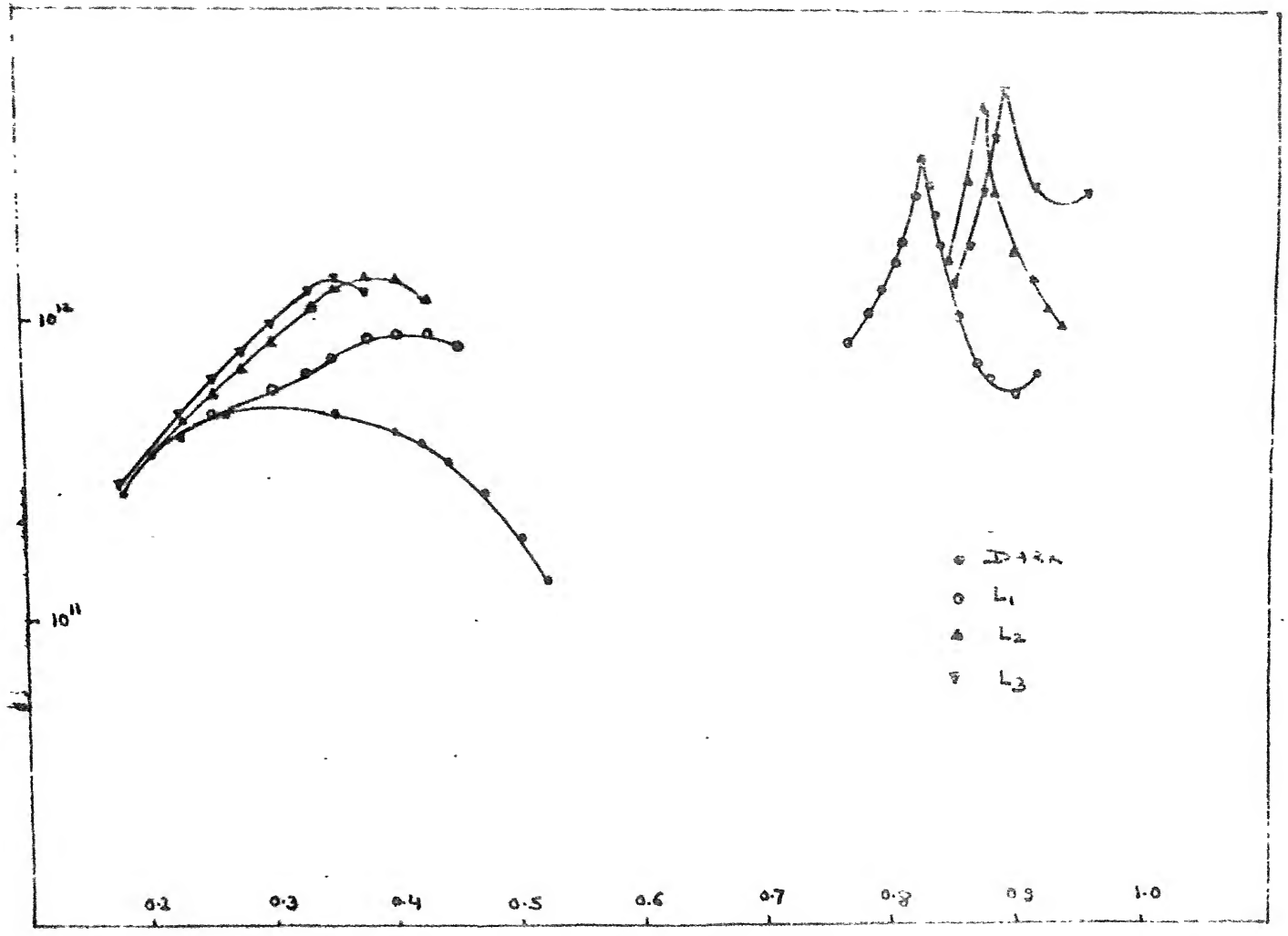

Fig. 4.9: Interface state density profile (capacitance method) in dark and [illegible]

the interface state profile, one near the valence band edge and the other near the conduction band edge in the lower band gap half.

The broad interface state peaks near the valence band edge can be identified as the inherent interface defects resulting from thermal oxidation of silicon as has been observed in the past experiments [13] and mentioned to be dominated by a broad peak centered around approximately 0.3 eV above the silicon valance band maximum.

This characteristic defect of thermal oxidation can be removed by employing a proper annealing and this yields the generally observed U shaped distribution [14].

In our work since no post oxidation annealing was done broad peaks around 0.3 - 0.4 eV above the valence band are observed in the profile of Fig. 4.9.

As shown in the profile the peak in the upper band gap half for illumination level L_3 occured at around 0.22 eV below the conduction band edge. This peak is similar to one obtained in the previous experiments and reported in the literature [10,15] to be due to defects introduced by irradiation. Rosencher et.al. [15] found that the defects introduced by Electron Beam give rise to a sharp set of levels below the conduction band with a very low electron capture cross section. These results differ from those obtained by Scoggan and Ma [10] who observed a broad

band near (E_c - 0.3) eV. This disagreement was partly attributed to the presence of surface potential fluctuations. The peaks obtained by us were quite sharp and were located within about 0.8 - 0.95 eV above the valence band as shown in Fig. 4.9 depending upon the illumination level employed.

In addition to the study of radiation defects due to Electron-Beam, defects due to other processes causing irradiation of the MOS structures have been explored in the past studies. Sinha [16] observed that the triode sputter etch cleaning step introduces surface states whose distribution shows a peak in the upper half of the band gap. The surface states and the oxide charge resulting from the damage were shown to be completely annealable using hydrogen. H_2 was trapped in SiO_2 prior to metallization and a low temperature inert ambient anneal was used subsequent to final deposition which caused redistribution of H_2 neutralizing surface states at the Si/SiO_2 interface.

The origin of these interface states might be due to the holes trapped at the $Si-SiO_2$ interface generated in the oxide by the Electron Beam Irradiation and the subsequent capture of injected electrons by these holes [6]. Winkour et.al. [9] explained the effect by release of energy by trapped holes may be on recombination with electrons, the released energy being sufficient to break bonds to give rise to the observed interface state peak.

This peak in the interface density profile due to radiation defect can be further explained on the basis of a positive ion release in the SiO_2 bulk via interactions with radiation generated holes and the subsequent transport of the librated ions to the SiO_2/Si interface as was proposed by Mclean [8]. The induced interface states result from an interaction of the ions at the surface.

Since the radiation dose to our sample was quite small, it was rather a 'stray' radiation incident on the sample and generated out of the E-Beam (from 2 kW E - Gun) striking the In_2O_3 target, the increase in interface state density due to irradiation is expected to be proportional to the pre-radiation density of the states since level of irradiation in our case is certainly below the high dose level as mentioned by Ma et al [7].

If the interface state profile at various illuminations is looked upon it can be seen that as the illumination intensity is increased the peaks in the state density profile also increase in magnitude and the peaks near the conduction and valence bands shift towards the respective bands. The reason as to why the state density increases with illumination and the shifting of the peaks to the respective carrier bands is not ascertained yet, and this has quite a wider scope for further investigation. Another relevant aspect in the further study might be the nature of these radiation induced interface states which as investigated by Scoggen and Ma [10] are donor type in the lower band gap half and acceptor type in the upper half of the band gap.

In a recent study Henderson [11] observed the optical dependence of P_b centres which are identified as triply coordinated silicon with a dangling bond and found them to increase with illumination. This may lead to the conclusion that triply coordinated silicon with dangling bond may be the source of the interface states.

The G_p/ω , G/f vs. frequency curves for minority and majority carriers for illumination L_3 are shown in Fig. 4.4 - 4.7, for majority carriers in dark are shown in Fig. 4.10 to 4.11.

For majority carriers i.e. holes as bias is increased in negative direction the G_p/ω peaks shift towards higher frequencies and vice versa for minority carriers i.e. holes. The interface state density profile obtained by conductance method is shown in Fig. 4.12 and is seen to be quite agreeable to that obtained by the capacitance technique. The profile for L_1 could not be obtained because the corresponding G_p/ω curve did not show any peak in the measurement range. Similarly no peaks were obtained corresponding to minority carriers under the illumination level L_1.

The capture cross section of holes was found to be about two orders of magnitude greater than the electron capture cross-section and the capture cross section is found to be illumination dependent and vary with band energy as shown in Fig. 4.13.

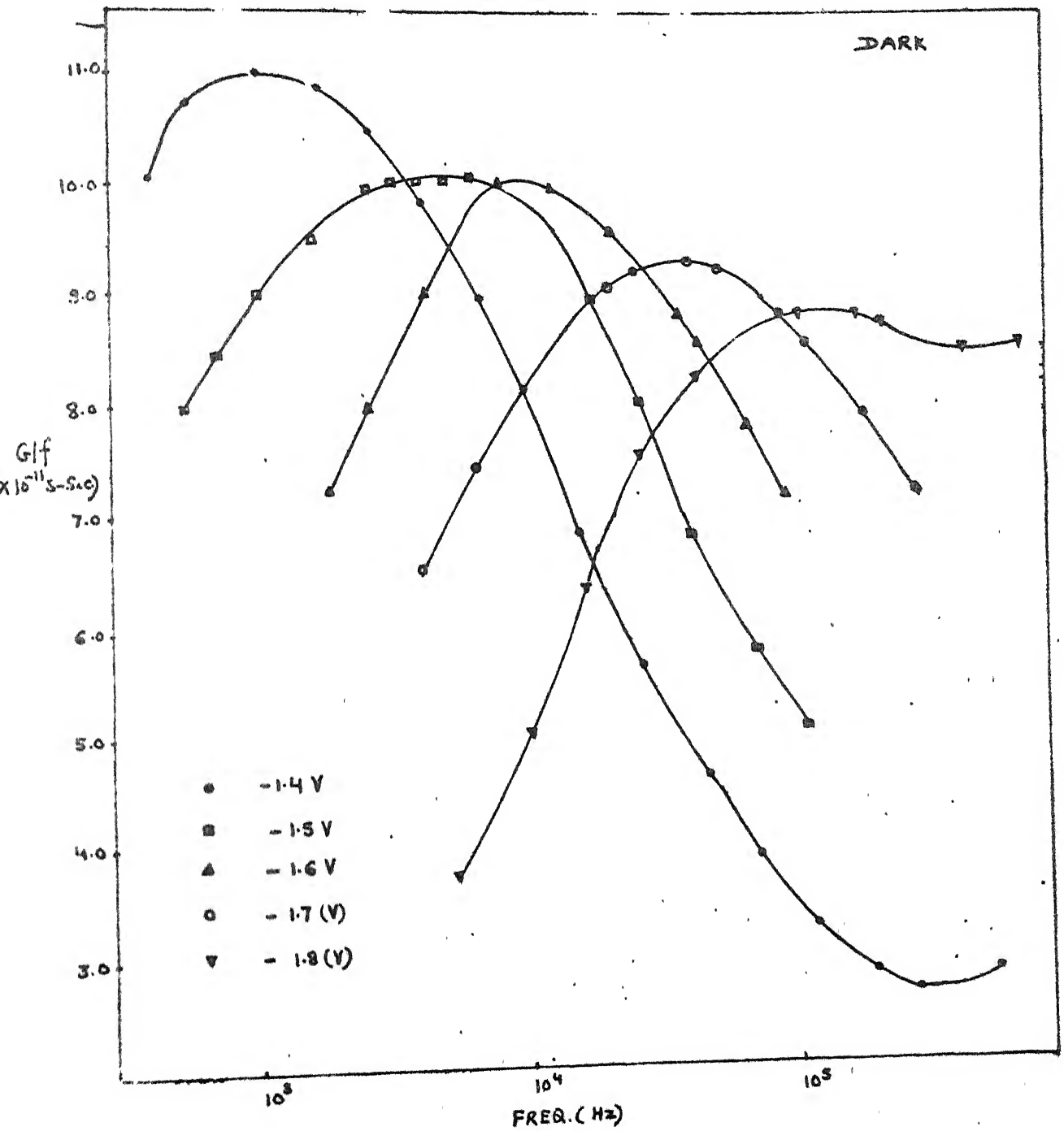

Fig. 4.10: G/f vs. f plot for the structure in dark.

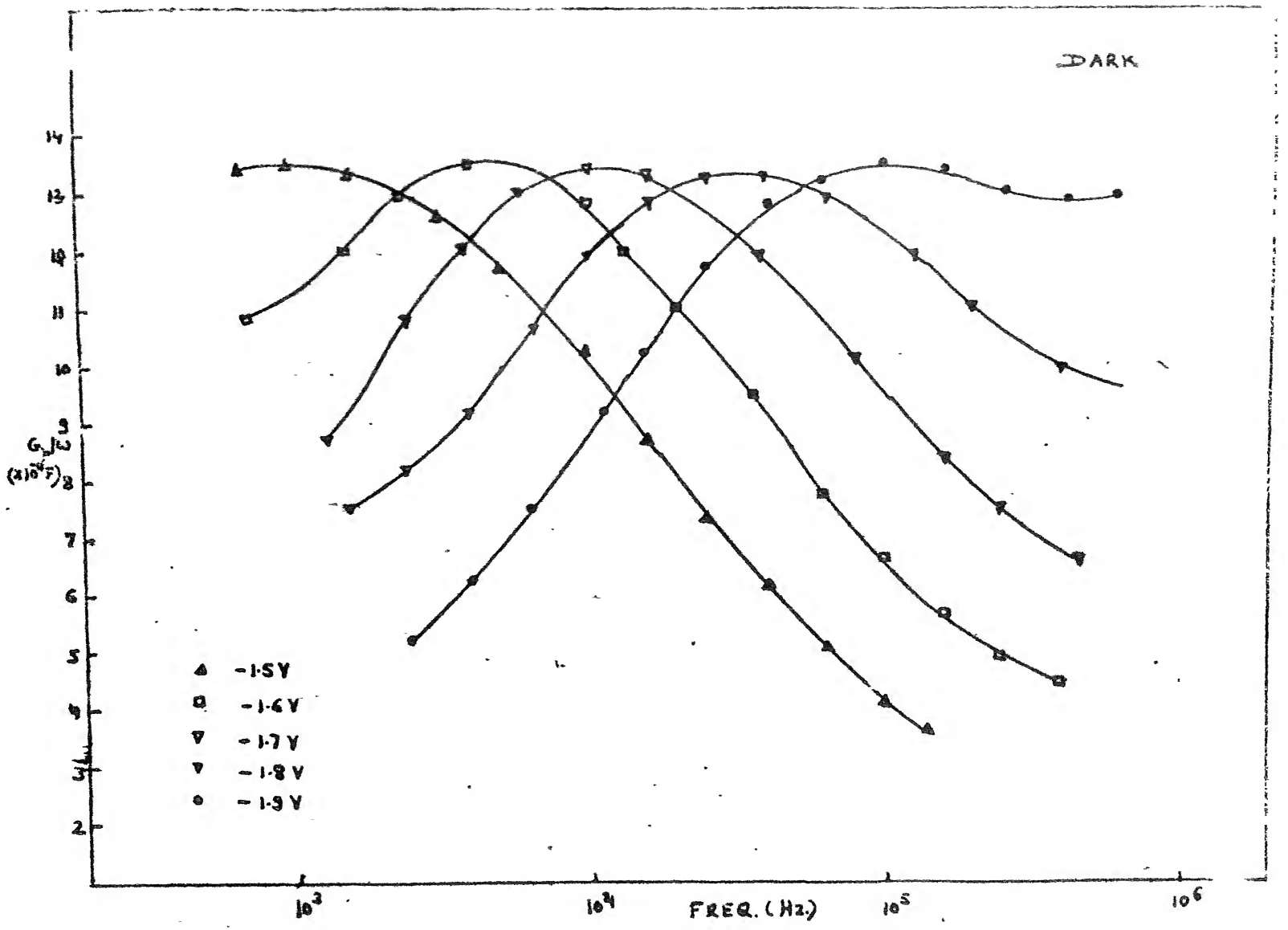

Fig. 4.11: C_p/ω vs. f plot for majority carrier peaks under dark condition.

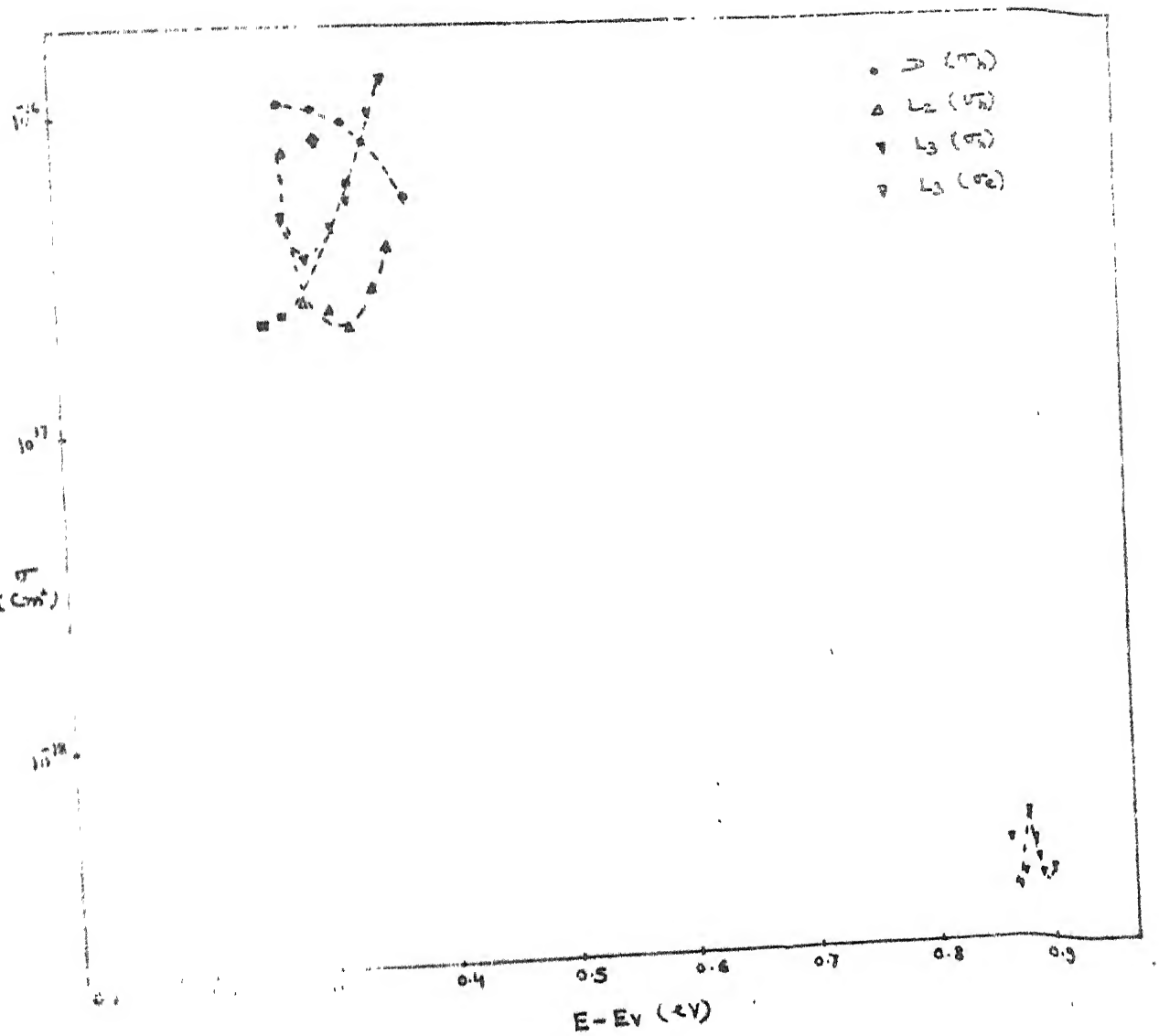

Fig. 4.13: Capture cross section vs. Energy plot in dark and under illumination levels L_1, L_2 and L_3 for electrons and holes.

Although the radiation induced damage can be reduced considerably by proper annealing, a control over both surface states and the fixed charge is possible by imploying higher deposition temperatures even though the deposition temperature may be lower than the post metallization annealing temperatures [12]

REFERENCES

1. S.M. Szi, Phys. of Semicond. Devices, (Wiley, New York), 1981.

2. C.N. Berglund, IEEE Trans. On Elect. Div. ED-13, 701 (1966).

3. S. Kar, S. Varma to be published.

4. S. Kar and S. Varma, J. Appl. Phy., 54, 1988 (1983).

5. E.H. Nicollian and A. Goetzberger, Bell Syst. Tech.J. 46, 1055 (1967).

6. S.K. Lai, Appl. Phys. Lett. 39, 58 (1981).

7. T.P. Ma, G. Scoggan, R. Leora, Appl. Phy.Latt.27,61 (1975).

8. F.B. Mclean, IEEE Trans. Nucl. Sc. Vol. NS-27, p. 1651 Dec. 1981.

9. P.S. Winkour et al, J. Appl. Phy. 50, 3492 (1979).

10. G.A. Scoggan and T.P. Ma, J. Appl. Phys. 48, 294 (1977).

11. B. Henderson, Appl. Phys. Lett., 44, 228 (1984).

12. M. Hamasaki, S.S. Elect. Vol. 26, No. 4, p. 299 (1983).

13. N.M. Johnson, D.J. Bartelink, and J.P. Mc Yittie, J. Vac. Sci and Technol. 16, 1407 (1979).

14. N.M. Johnson, D.K. Biegelsen and M.D. Moyer, The Physics of MOS Insulators, (Pergamon, New York, 1980), p.311.

15. E. Rosencher, A. Chantre and D. Bois, The Physics of MOS Insulators, (Pergamon, New York, 1980), p. 331.

16. A.K. Sinha, J. Electrochem. Soc. 123, 65 (1976).

CHAPTER V

CONCLUSION

In our present work the damages due to Electron-Beam radiation produced in the MOS structures were investigated. The study was carried over the $Si/SiO_2/In_2O_3$ structure whose top transparent gate was deposited using the Electron-Beam evaporation.

The interface investigation was done with the help of both the capacitance as well as the conductance technique and the interface state density profiles obtained by both the techniques agreed well with each other. Employing a uniform background of illumination for three different intensities helped in accessing the minority carrier band gap half for the determination of interface state density and the capture cross section.

The investigation of interface state density along the band gap showed the presence of two peaks, one near the valence band edge and the other near the conduction band edge. The peak near the valence band edge, an inherent characteristic of the thermal oxidation process was a broad one and located approximately 0.3 eV above the valence band. The peak near the conduction band edge, induced due to the damage caused by the

Electron-Beam irradiation was a sharp one and located in the energy range of 0.8 to 0.95 eV above the valence band depending upon the intensity of illumination employed.

Both the peaks were found to shift towards the respective band edges with increase in illumination and also the peak value found to increase.

The mechanism involved in the above behaviour of interface state density is not understood well. Whether the increase in density is due to the reversible defects induced because of photons or, the apparent increase is seen as a result of enhancement in charging of interface states in the presence of photons is still an unexplained issue.

Validity of considering 1 MHz as the high frequency was checked and it was found quite suitable.

The quasi Fermi level separation found by the parallel shift method and the high frequency minimum method quite well agreed with each other while the integration method yielded higher value possibly because of insufficient band bending at the integration limit points in strong accumulation and inversion.